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43	FAN	0.1	
44	LED	0.1	
45	DB CONN (PSwitch/PSP/IO)	0.1	
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54	AUDIO(CODEC & POWER)	0.1	
55	AUDIO DSP	0.1	
56	AUDIO(HP)	0.1	
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61	Power Block Diagram	0.1	
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65	DDR2PWR(+1_8V/+0_9V)	0.1	
66	SYSPWR(+1_1V/+1_5V)	0.1	
67	SYSPWR(+1_2V)	0.1	
68	VHCORE (1) -- ISL6334A	0.1	
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70	OVP Protect	0.1	
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74	Power Sequence Timing	0.1	
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FUBAI PCB P/N: 1P-0089J00-80SA

P. Leader	Check by	Design by

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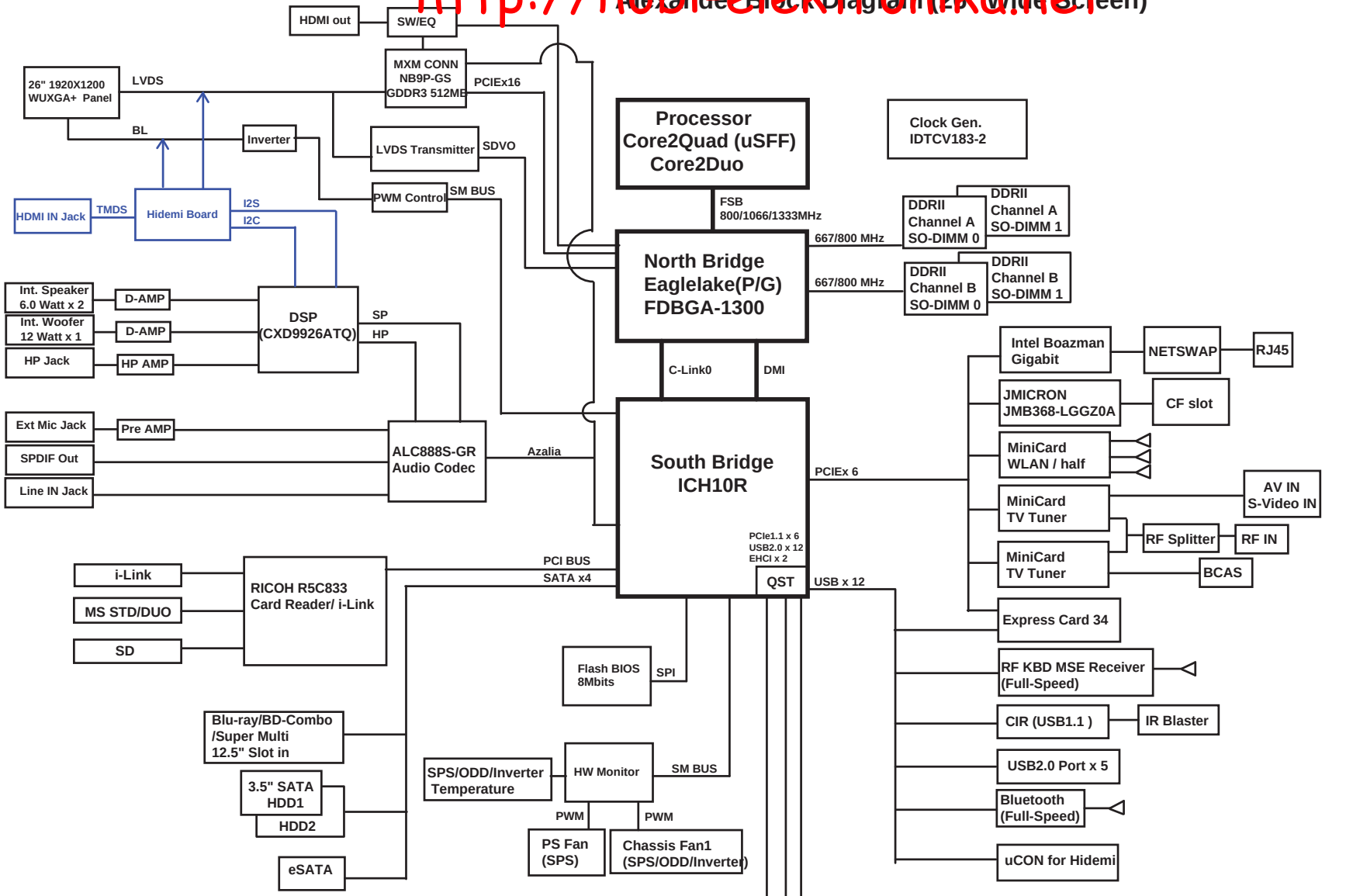
Alexander Block Diagram (26" Wide Screen)



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4/7For corwin spring

7/10Change C11,C12 from 1C-2N20270-J000 to 1C-2N20300-J600

1. Clock Request Table

FSC	FSB	FSA	CPU	SRC[7:0]	PCI	USB	DOT	REF
1	0	0	333.33	100	33	48	96	14.318
0	0	0	266.66	100	33	48	96	14.318
0	1	0	200	100	33	48	96	14.318

	Clock Request	Clock Request Function	Clock Output	BYTE	BIT	1	BYTE	BIT	1
PIN 1	PCI0/CR#_A	SATACLKREQ#	SRC2	5	7	CR#_A mode	5	6	SRC2
PIN 3	PCI1/CR#_B	EXPRESS_DET#	SRC4	5	4	CR#_A mode	5	7	SRC4
PIN 32	SRCC11/CR#_G	TUNER2_DET#	SRC9	6	5	CR#_G mode Control SRC9			
PIN 33	SRCT11/CR#_H	TUNER1_DET#	SRC10	6	4	CR#_G mode Control SRC10			

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Title: CLOCK GEN

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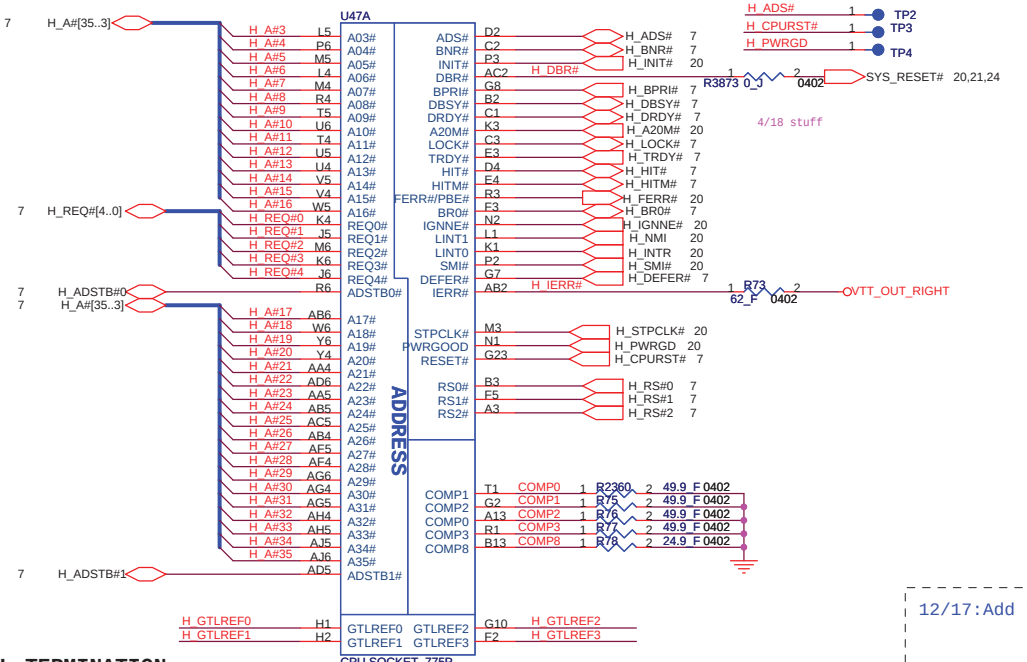
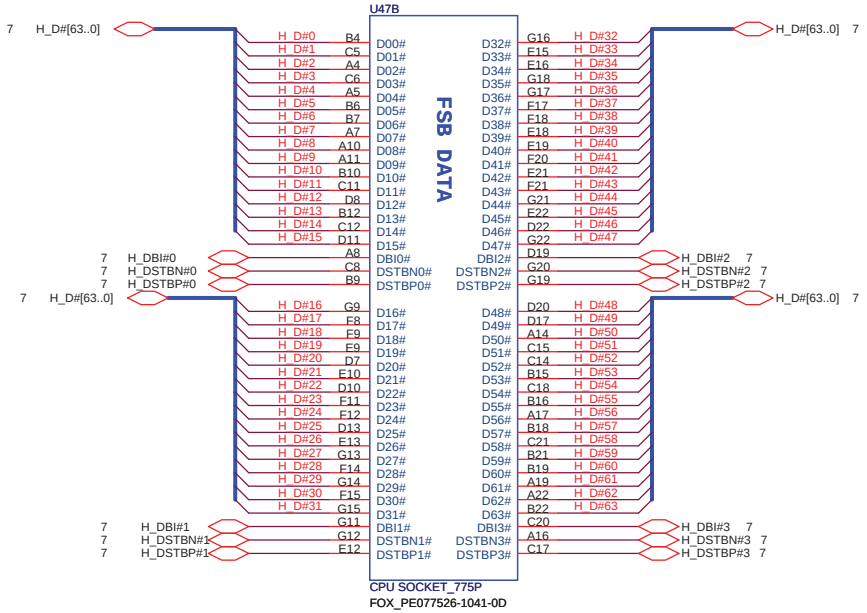
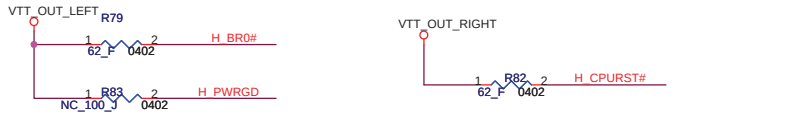
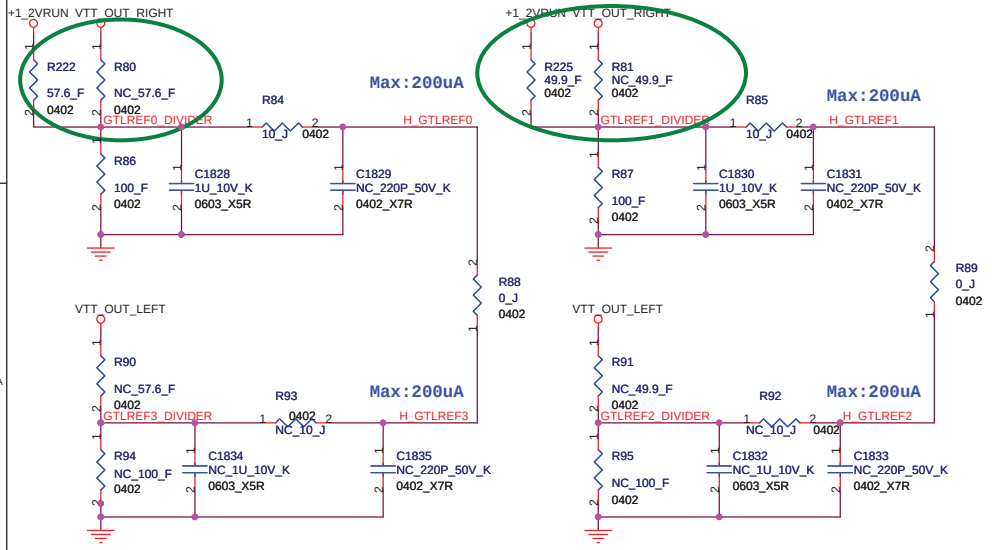


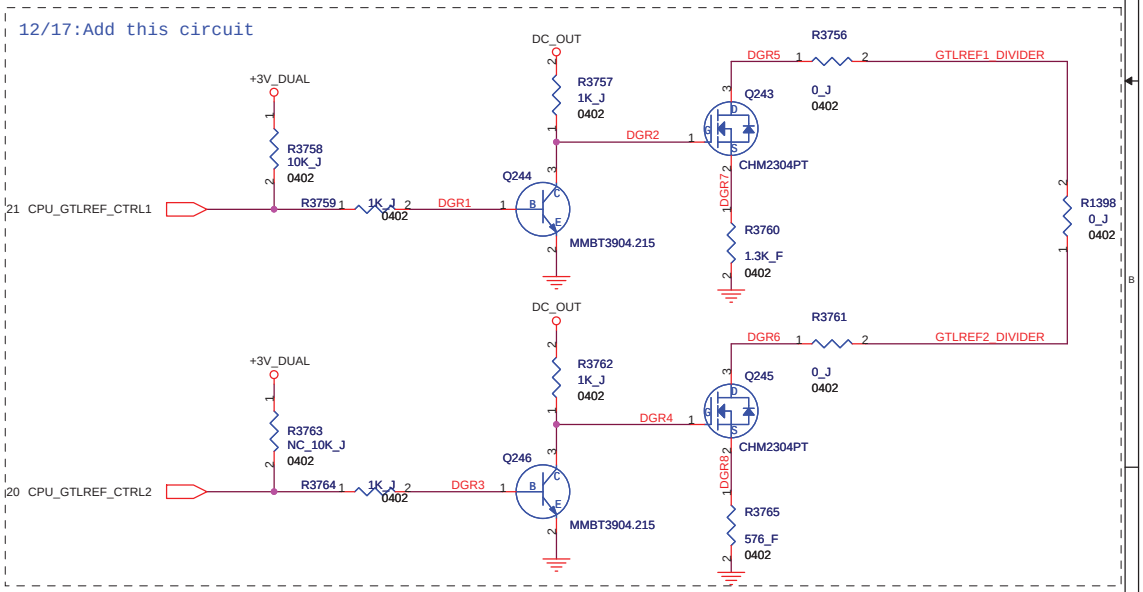


CPU SIGNAL TERMINATION



Layout note : Please near the proccessor





GTLREF FUNCTION TABLE

CPU_GTLREF_CTRL2	CPU_GTLREF_CTRL1	Ratio Set
0	0	0.615 X VTT
0	1	0.63 X VTT
1	0	0.65 X VTT
1	1	0.67 X VTT

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Title: CPU HOST

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VTT(1.045v~1.145v,Typ 1.1V):
Wolfdale--max 4.6A
Yorkfied--max 8A

U47C

TP5 TP_SKTOCC# AE8 SKTOCC#

MSID0 MSID1 VRDSEL
W1 TP_MSID0 — TP6
V1 TP_MSID1 — TP7
AL3 TP_VRDSEL — TP12

20 H_PECI G5
20,21,50 H_THERMTRIP# M2
H_PROCHOT# AL2
TP10 TP_THERMDA AL1
TP11 TP_THERMDC AK1

PECI THERMTRIP# PROCHOT# THERMDA THERMDC

THRM

FC

FC0 FC3 T2 FC4 AK6 E24 H29 Y3 AE3 E5 F6 J3 A24 E29 U2 U3 J16 H15 H16 J17 H4 AD3 AB3 AA2 AM6

Y1 FC0 51_J R103 0402
J2 TP_FC3 — TP13
PM_DPRSTP# 8,21
TP_FC8 — TP14
TP_FC10 — TP15
TP_FC15 — TP16
TP_FC17 R104 NC_0_J 0402 PSI# 68
TP_FC18 — TP18
TP_FC20 — TP19
IMPSEL
TP_FC22 — TP21
TP_FC23 — TP23
TP_FC26 — TP25
TP_FC29 — TP26
TP_FC30 — TP27
TP_FC31 — TP28
TP_FC32 — TP29
TP_FC33 — TP30
TP_FC34 — TP31
TP_FC35 — TP32
TP_FC36 — TP33
TP_FC37 — TP34
TP_FC39 — TP35
VRMPWRGD_CPU 26

IMPSEL — R105 51_J 0402

TESTHI_0 F26
TESTHI_1 W3
TESTHI_2_7 F25 G25 G27 G26 G24 F24
TESTHI_10 H5
20 DPSLP# P1
8 PM_SLP# L2

TESTHI

TESTHI00 TESTHI01 TESTHI02 TESTHI03 TESTHI04 TESTHI05 TESTHI06 TESTHI07 TESTHI10 TESTHI11 TESTHI13

TP36 TP_CPU_RESERVED V2
TP38 TP_CPU_RSVD1 N4
TP40 TP_CPU_RSVD2 P5
TP42 TP_CPU_RSVD3 AC4
TP44 TP_CPU_RSVD4 AE4
TP46 TP_CPU_RSVD9 F29
TP48 TP_CPU_RSVD11 G6
TP50 TP_CPU_RSVD12 AH2
TP52 TP_CPU_RSVD13 N5

RESERVED RSVD1 RSVD2 RSVD3 RSVD4 RSVD9 RSVD11 RSVD12 RSVD13

RSV

RSVD14 RSVD17 RSVD18 RSVD19 RSVD21 RSVD31 RSVD33 RSVD34 RSVD35

AE6 TP_CPU_RSVD14 — TP37
D16 TP_CPU_RSVD17 — TP39
A20 TP_CPU_RSVD18 — TP41
F23 TP_CPU_RSVD19 — TP43
F23 TP_CPU_RSVD21 — TP45
E7 TP_CPU_RSVD31 — TP47
D14 TP_CPU_RSVD33 — TP49
E6 TP_CPU_RSVD34 — TP51
D1 TP_CPU_RSVD35 — TP53

CPU SOCKET_775P
FOX_PE077526-1041-0D

VTT_OUT_RIGHT

NC_62R_J R96 0402 TDO
62R_J R98 0402 TDI_M
62R_J R100 0402 TDI
62R_J R101 0402 TMS
62R_J R102 0402 TRST#

U47D

TDO TDI_M TDI TMS TRST#

XDP

TDO_M TCK ITPCLKOUT0 ITPCLKOUT1

AE1 TDO
W2 TDI_M
AD1 TDI
AC1 TMS
AG1 TRST#

U1 TDO_M NC_62_F1 R97 0402
AE1 TCK 62_F R99 0402
AK3 XDP_CLKOUT_DP — TP8
AJ3 XDP_CLKOUT_DN — TP9

XDP_BPMb0# G1
XDP_BPMb1# C9
XDP_BPMb2# G4
XDP_BPMb3# G3

BPMb0# BPMb1# BPMb2# BPMb3#

BPM0# BPM1# BPM2# BPM3# BPM4# BPM5#

AJ2 XDP_BPM0#
AJ1 XDP_BPM1#
AD2 XDP_BPM2#
AG2 XDP_BPM3#
AF2 XDP_BPM4#
AG3 XDP_BPM5#

TP20 TP_VCCA A23
TP22 TP_VSSA B23
HVCCPLL D23
TP24 TP_VCCIOPLL C23
0_J R106 H_VCC_MB_REG AN5
0_J R107 H_VSS_MB_REG AN6
0402 VSS_SENSE_H AN4
VCC_SENSE_H AN3

68 VCC_SENSE
68 VSS_SENSE

VCCA VSSA VCCPLL VCCIOPLL VCC_MB_REG VSS_MB_REG VSSSENSE VCCSENSE

VID_SELECT

AN7 CPU_VID_SELECT — TP203

VID0 VID1 VID2 VID3 VID4 VID5 VID6 VID7

AM2 AL5 AM3 AL6 AK4 AL4 AM5 AM7

VID0 68
VID1 68
VID2 68
VID3 68
VID4 68
VID5 68
VID6 68
VID7 68

TP195 TP_VTT_SEL F27
J1
AA1

VTT_SEL VTT_OUT_LEFT VTT_OUT_RIGHT

VTT_OUT_RIGHT
VTT_OUT_LEFT

C32 0.1U_16V_K 0402_X7R
C33 0.1U_16V_K 0402_X7R
C34 NC_0.1U_16V_K 0402_X7R

FSBSEL0 3,8
FSBSEL1 3,8
FSBSEL2 3,8

FSBSEL0 G29
FSBSEL1 H30
FSBSEL2 G30

BSEL0 BSEL1 BSEL2

BCLK0 BCLK1

F28 CK_CPU_P 3
G28 CK_CPU_N 3

CPU SOCKET_775P
FOX_PE077526-1041-0D

+1_2VRUN

R121 51_J 0402 TESTHI_0
R123 51_J 0402 TESTHI_2_7

+1_5VRUN

placed within 500 mils of the CPU socket

R111 0_J 0603 Max:130mA HVCCPLL

C35 10U_10V_M 0805_X5R
C36 0.01U_10V_K 0402_X7R

VTT_OUT_RIGHT

R110 51_J 0402 XDP_BPM0#
R112 51_J 0402 XDP_BPM1#
R113 51_J 0402 XDP_BPM2#
R114 51_J 0402 XDP_BPM3#
R115 51_J 0402 XDP_BPM4#
R116 51_J 0402 XDP_BPM5#

VTT_OUT_LEFT

R122 NC_51_J 0402 XDP_BPMb1#
R124 51_J 0402 XDP_BPMb2#
R127 51_J 0402 XDP_BPMb3#
R119 0_J 0402 XDP_BPMb0#

12/22 Changed for No BPMb support
DG page 97

VTT_OUT_RIGHT

R134 NC_680_J 0402 CPU_VID_SELECT

12/22 Changed reference to DG page 98

VTT_OUT_LEFT

R37920 51_J 0402 TESTHI_1
R126 51_J 0402 TESTHI_10
R128 NC_51_J 0402 DPSLP#
R130 NC_51_J 0402 PM_SLP#
R133 NC_51_J 0402 PM_DPRSTP#

+1_2VRUN

R125 470_J 0402 FSBSEL0
R129 470_J 0402 FSBSEL1
R132 470_J 0402 FSBSEL2

VSS_SENSE R139 NC_0_J 0402 VSS_SENSE_H
VCC_SENSE R140 NC_0_J 0402 VCC_SENSE_H

VTT_OUT_RIGHT

R137 NC_130_F 0402

VR_HOT#

PQ53 2N7002PT

68 VR_HOT

+3VRUN

R37917 10K_J 0402

Q293 MMBT3904.215

Q292_G

Q292 MMBT3904.215

1K_J 0402

70 PWRLIMIT# R3874 LIMIT_G

H_PROCHOT#

R138 1K_J 0402

+3VRUN

R136 10K_J 0402

Q162 MMBT3904.215

PHOT_C

+3VRUN

R37910 10K_J 0402

ICH_THRM# — ICH_THRM# 21,42

Q163 MMBT3904.215

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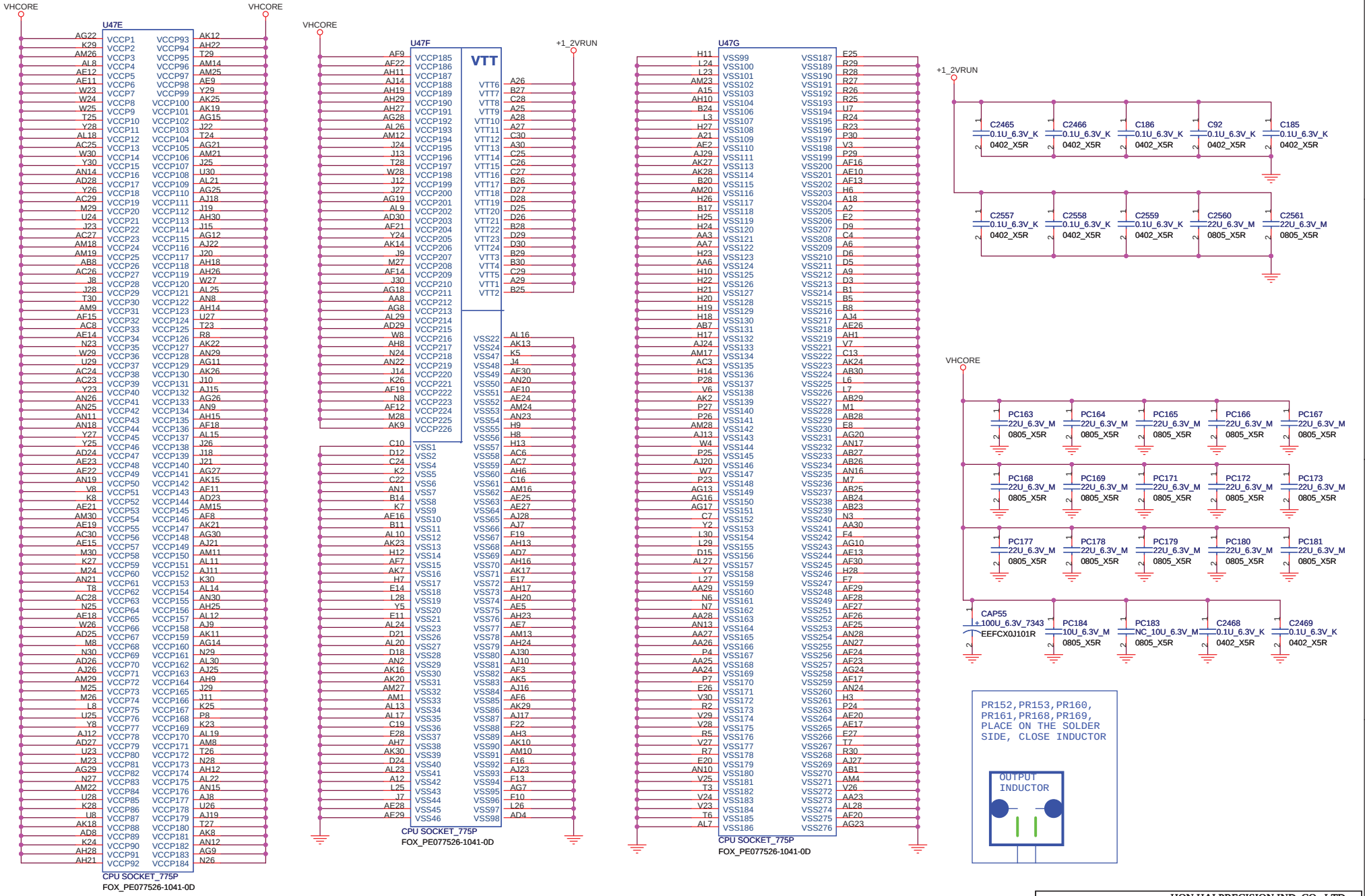
VHCORE(0.85V-1.45V,VCC_BOOT=1.1V):
Wolfdale--max 75A
Yorkfied--max 125A



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Title: CPU POWER		
Size: A3	Document Number: M841 DVT	Rev: 0.1
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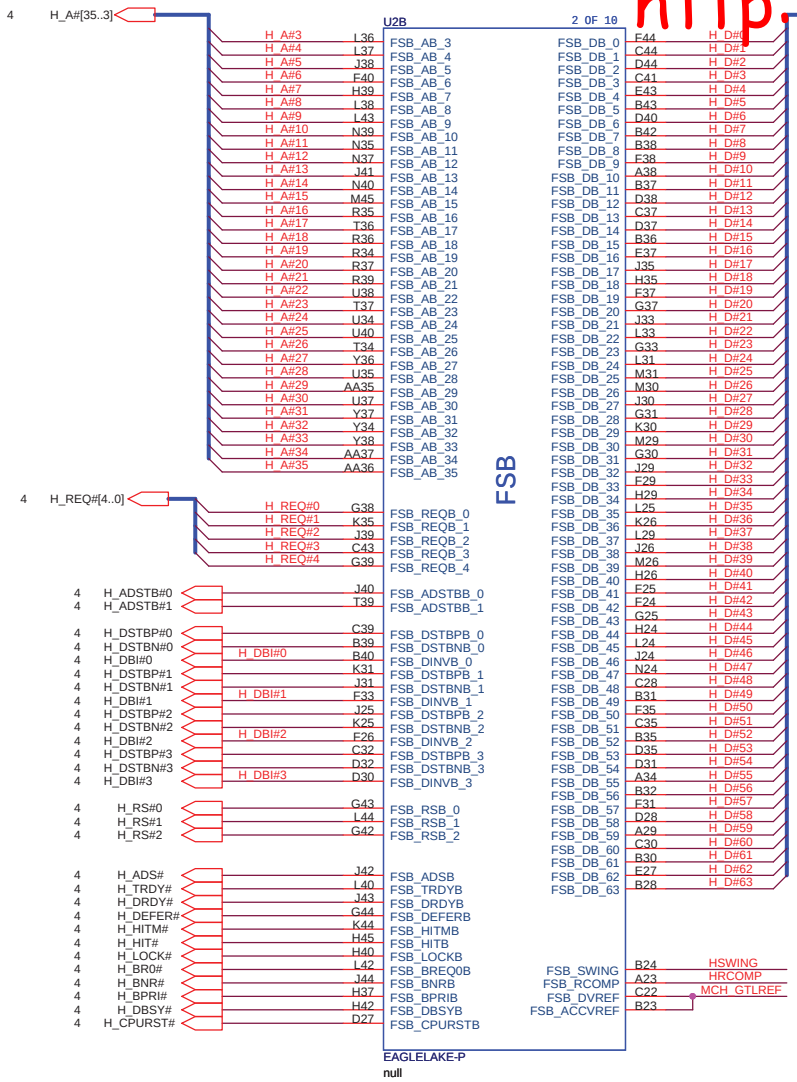

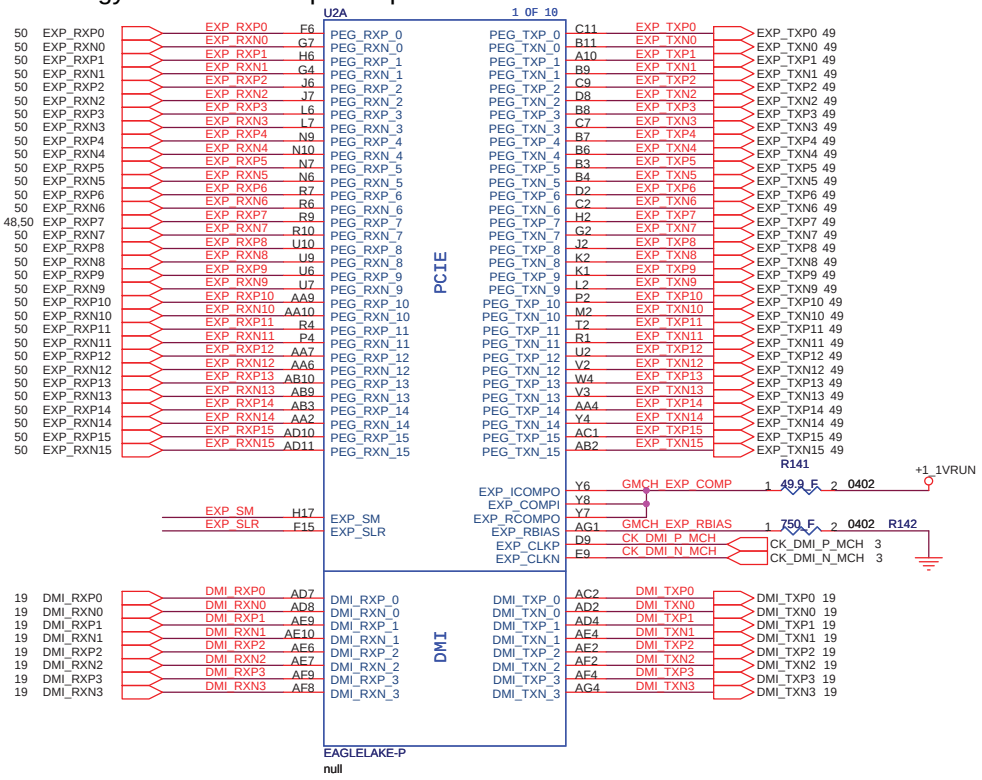

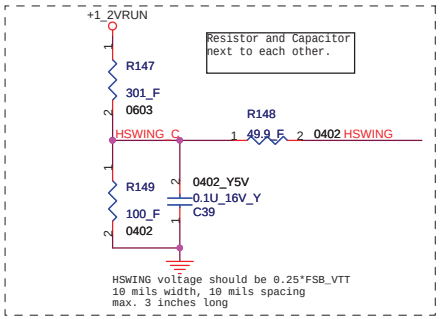

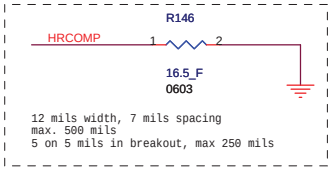

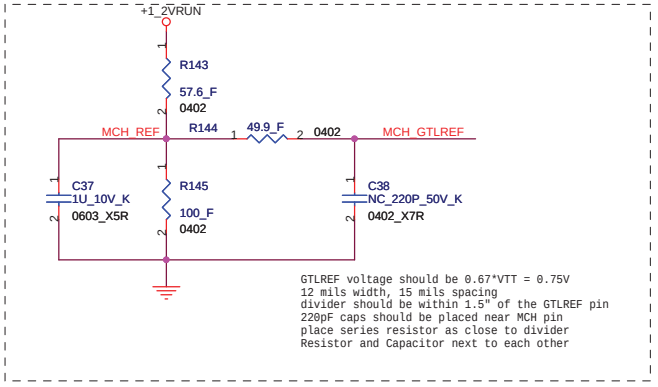

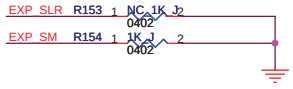

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Eaglelake HOST/PCI-E 1/7
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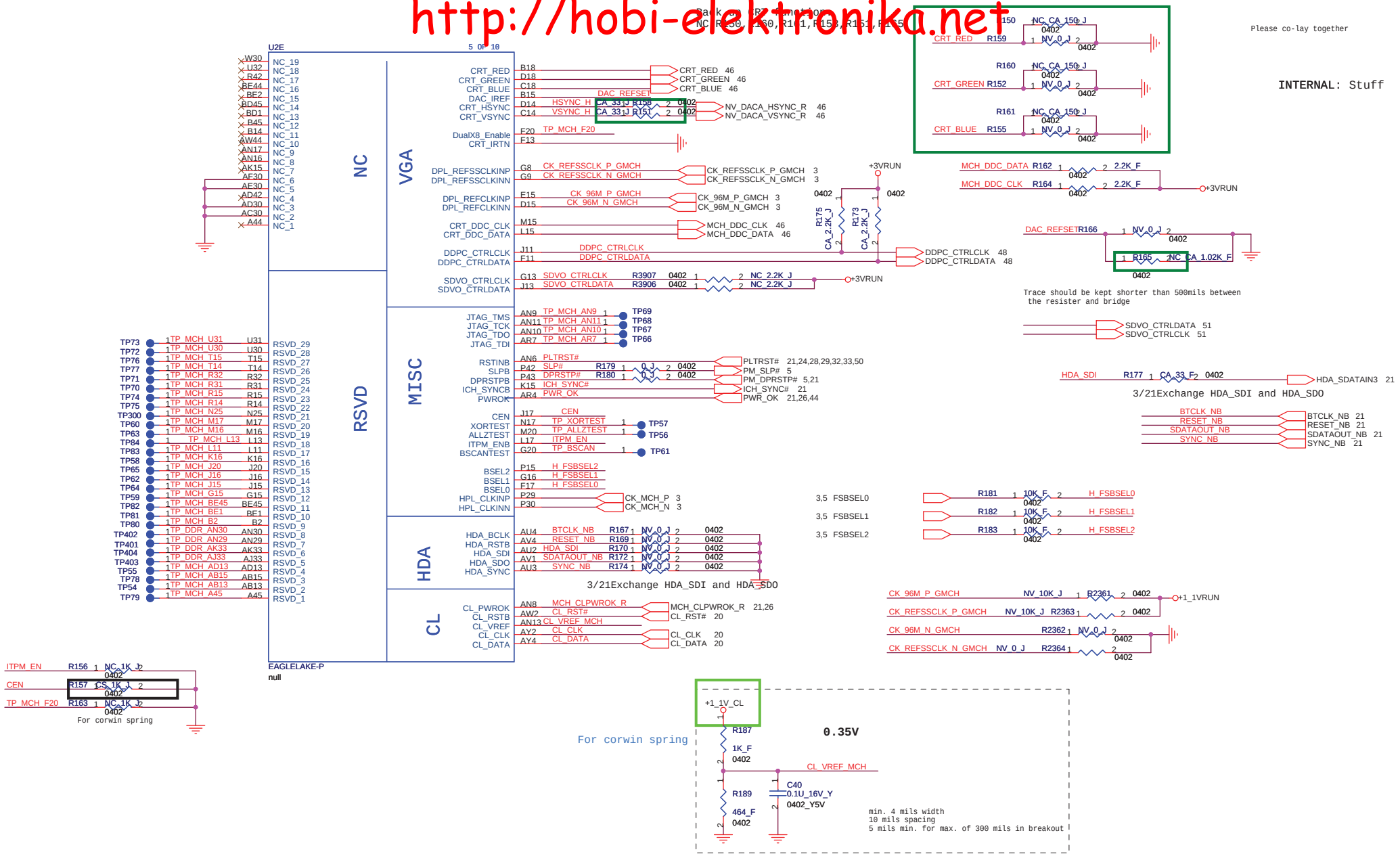

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Eaglelake VGA/MISC 2/7
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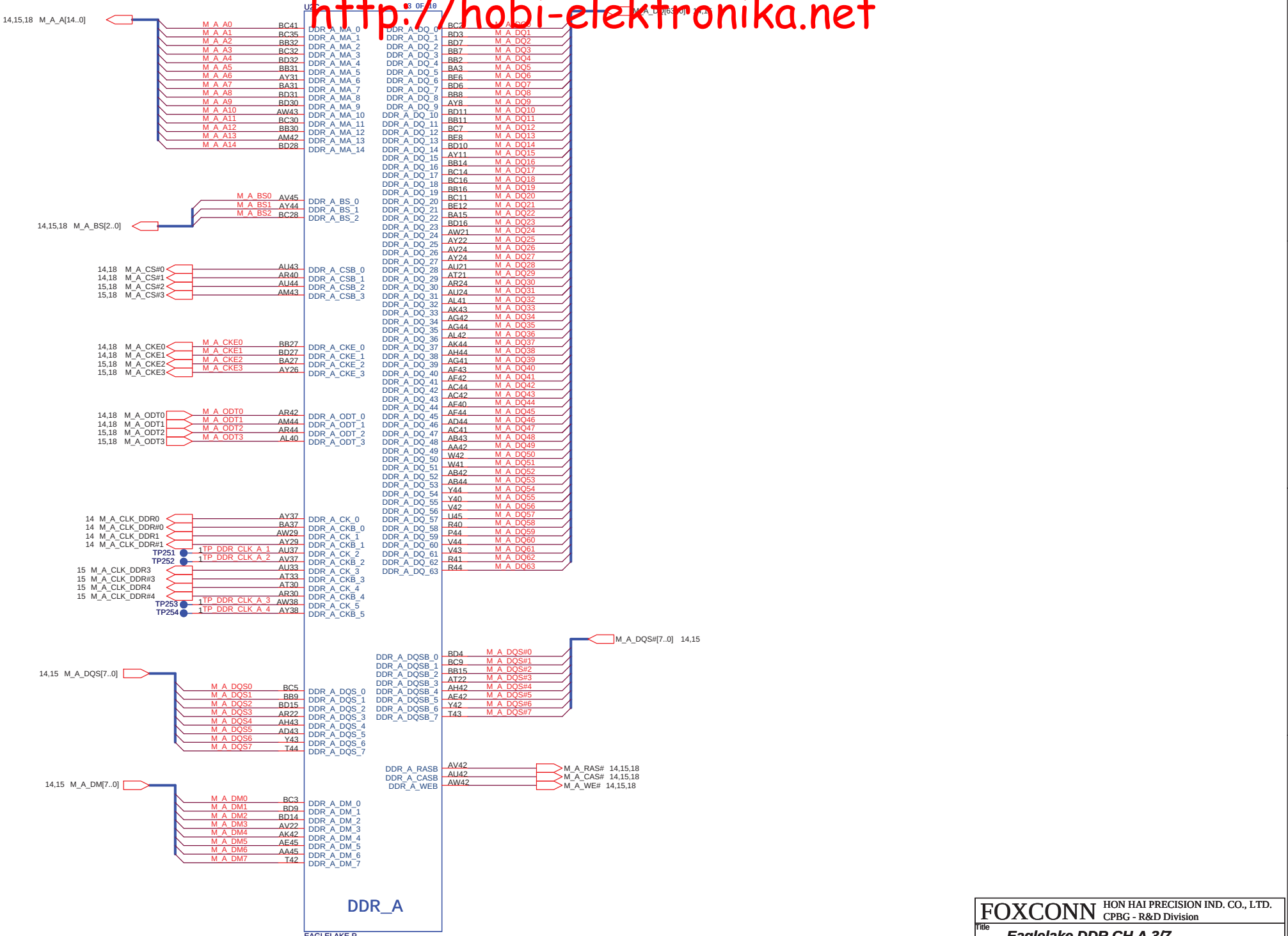

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Title: Eaglelake DDR CH A 3/7

Size	Document Number	Rev
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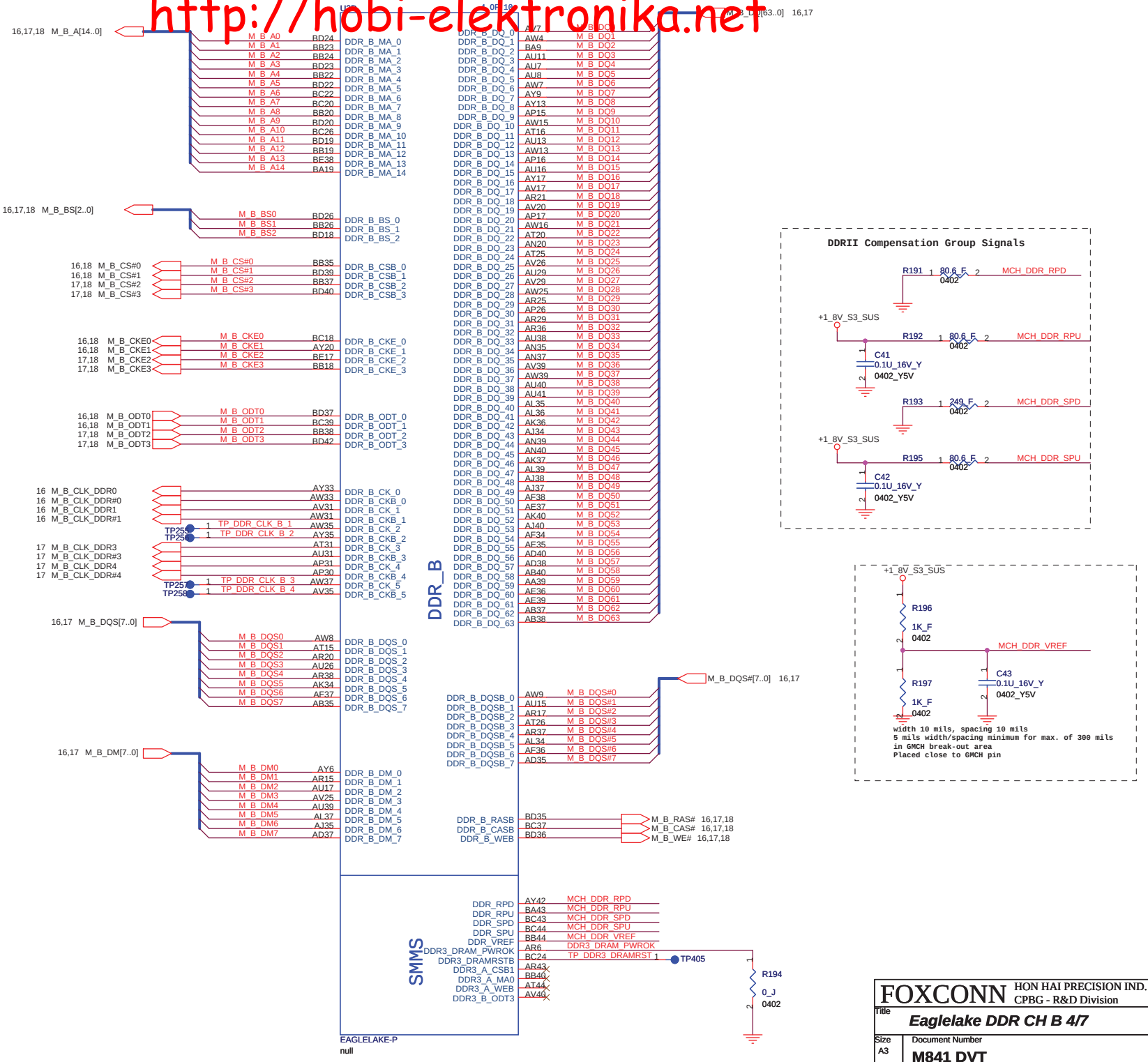

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Eaglelake DDR CH B 4/7	
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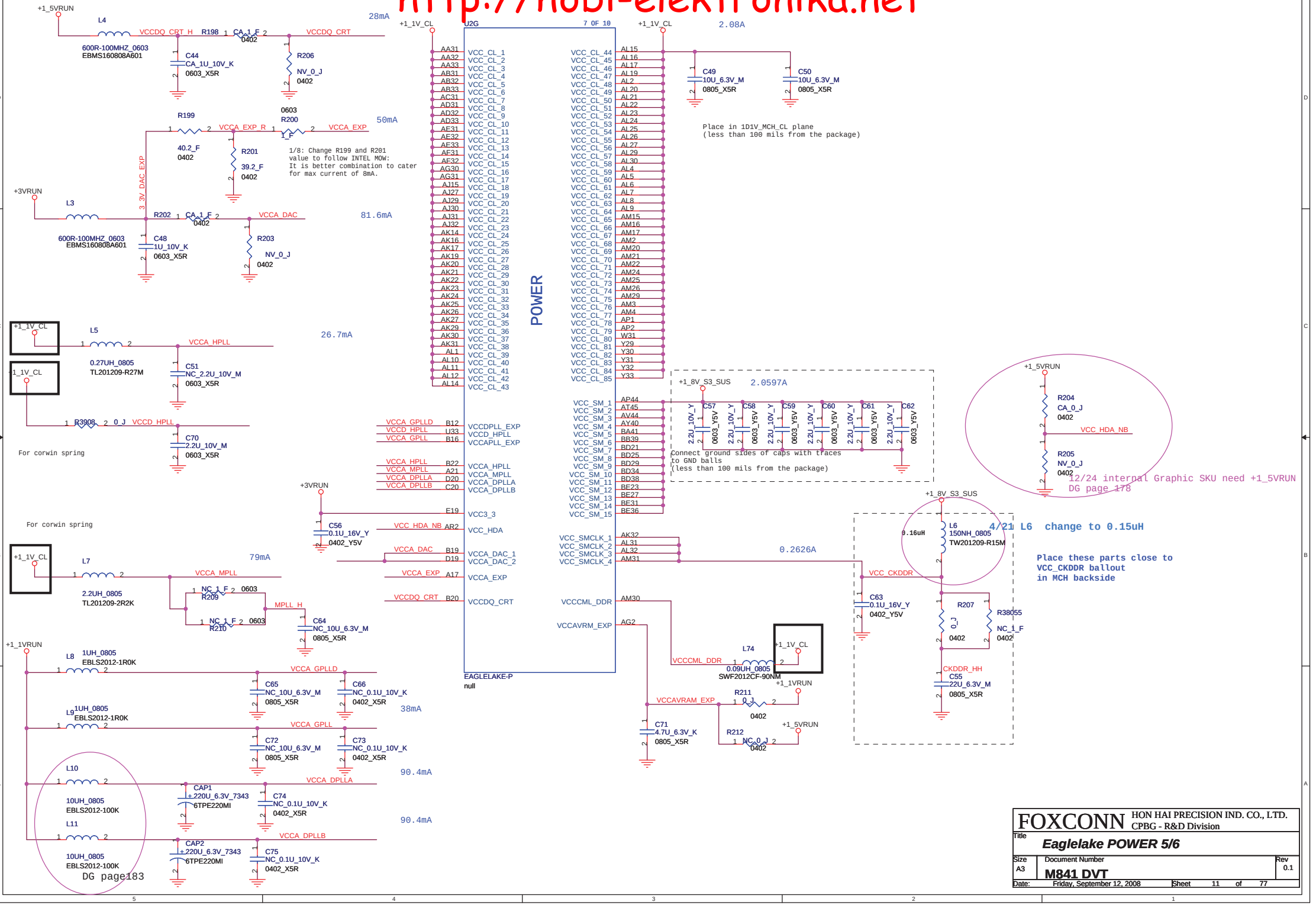

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Title	*Eaglelake POWER 5/6*		
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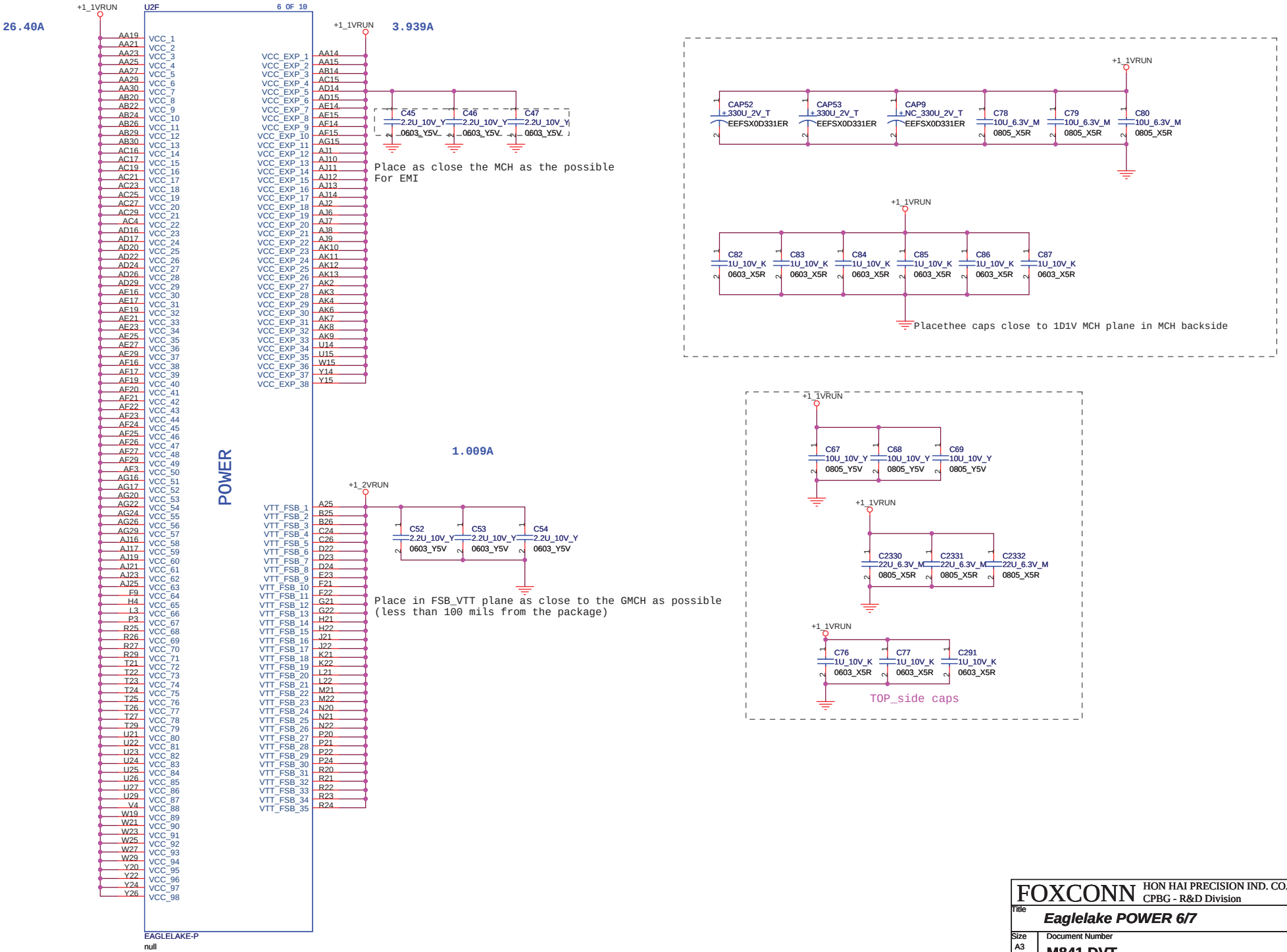

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Eaglelake POWER 6/7
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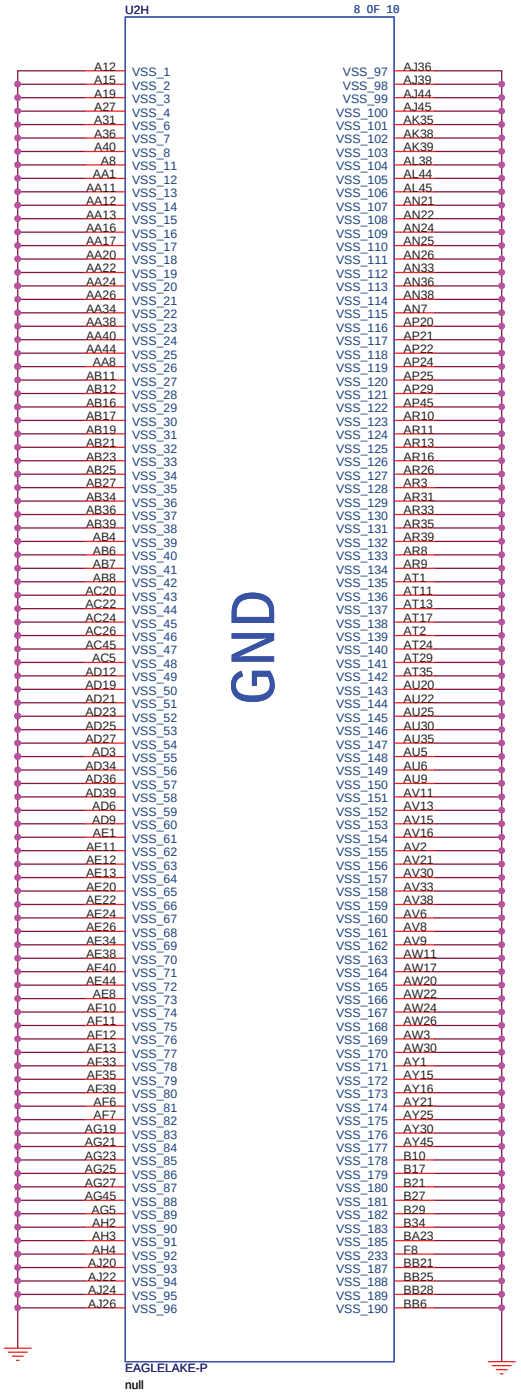

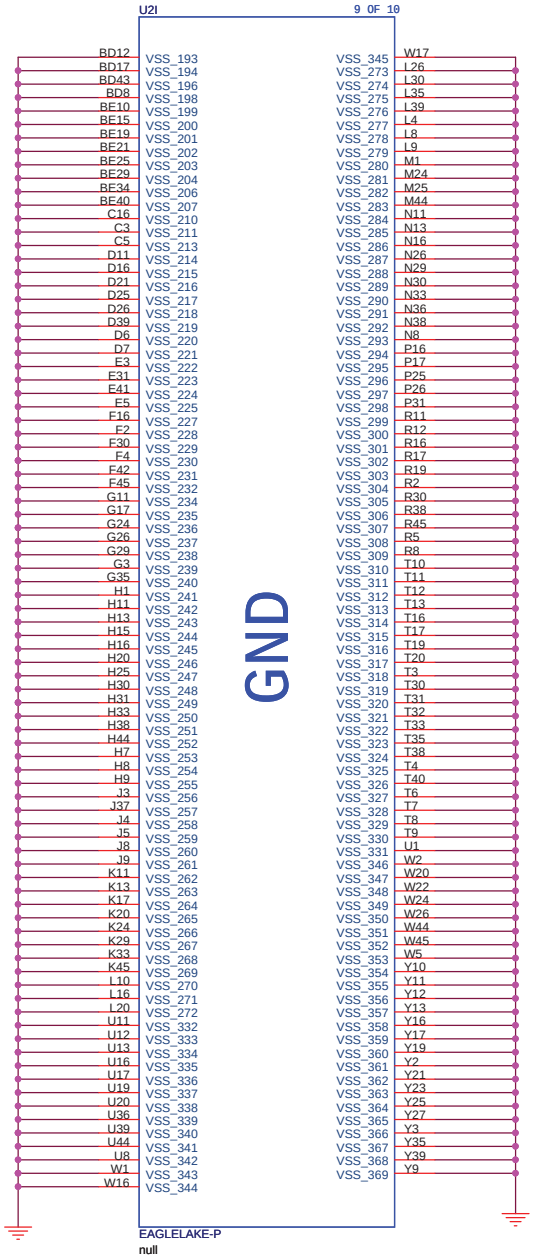

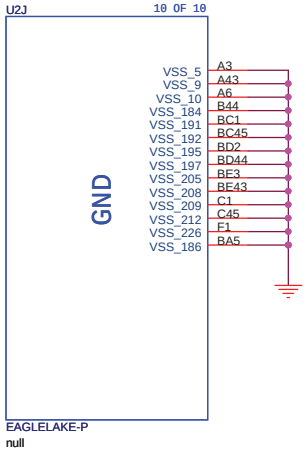

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	Eaglelake GND 7/7		
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1.8V per DIMM=3.08A

DDR2_VREF_A

C90 0.1U_16V_M 0402_X5R

C91 2.2U_10V_M 0603_X5R

0.1 µF and 2.2 µF placed close to VREF pins

+1_8V_S3_SUS

CN1

DDR2_200P
FOX_AS0A426-N2RN-4F

5.2mm

For corwin spring

C106 0.1U_6.3V_K 0402_X5R

SMB_DATA_SB
SMB_CLK_SB
VDD_SPD_A

SA0_A1 10K_J R217 0402
SA1_A1 10K_J R218 0402

DDR2_EXTTS#0 → TP259

M_A_CLK_DDR0 9
M_A_CLK_DDR#0 9
M_A_CLK_DDR1 9
M_A_CLK_DDR#1 9

M_A_CKE0 9,18
M_A_CKE1 9,18
M_A_BS2 9,15,18
M_A_A14 9,15,18
M_A_BS0 9,15,18
M_A_WE# 9,15,18
M_A_CAS# 9,15,18
M_A_CS#1 9,18
M_A_CS#0 9,18
M_A_ODT1 9,18
M_A_ODT0 9,18

M_A_DM[7..0] 9,15
M_A_DQ[63..0] 9,15
M_A_DQS[7..0] 9,15
M_A_DQS#[7..0] 9,15
M_A_A[14..0] 9,15,18

DDRDIMM_VREF
DDR2_VREF_A
(20 mil)

R108 NC_0_J 0402
R214 1K_D 0402
R215 910_D 0402
C102 0.1U_16V_Y 0402_Y5V

Close to DIMM

+1_8V_S3_SUS
CAP10 ±330U_6.3V_M 7.3x4.3x2.8

+0_9VRUN
C2366 4.7U_6.3V_K 0603_X5R
C2367 4.7U_6.3V_K 0603_X5R

1/1 changed from +1_8_S3_SUS to +0_9RUN

C93 1U_10V_K 0402_X5R
C94 1U_10V_K 0402_X5R
C95 1U_10V_K 0402_X5R
C96 1U_10V_K 0402_X5R

Place these Caps near Channel A Dimm0 power pin

Place these Caps near So-Dimm0.

C98 0.1U_16V_Y 0402_Y5V
C99 0.1U_16V_Y 0402_Y5V
C100 0.1U_16V_Y 0402_Y5V
C101 0.1U_16V_Y 0402_Y5V

For corwin spring

R178 CS_0_J 0402 +3_3V_CL
R184 NCS_0_J 0402 +3VRUN
15 VDD_SPD_A

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
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1.8V per DIMM=3.08A

DDR2_VREF_A

+1_8V_S3_SUS

+1_8V_S3_SUS

C107 0.1U_16V_M 0402_X5R

C108 2.2U_10V_M 0603_X5R

0.1 µF and 2.2 µF placed close to VREF pins

CN2

DDR2 SDRAM SO-DIMM (200P)

9.2mm

DDR2_200P

FOX_AS0A426-NARN-4F

M_A_DM[7..0] 9,14

M_A_DQ[63..0] 9,14

M_A_DQS[7..0] 9,14

M_A_DQS#[7..0] 9,14

M_A_A[14..0] 9,14,18

M_A_CLK_DDR3 9

M_A_CLK_DDR#3 9

M_A_CLK_DDR4 9

M_A_CLK_DDR#4 9

DDR2_EXTTS#1 1 TP260

M_A_CKE2 9,18

M_A_CKE3 9,18

M_A_BS2 9,14,18

M_A_A14 9,14,18

M_A_BS1 9,14,18

M_A_RAS# 9,14,18

M_A_CS#2 9,18

M_A_ODT2 9,18

M_A_A13

M_A_BS0 9,14,18

M_A_WE# 9,14,18

M_A_CAS# 9,14,18

M_A_CS#3 9,18

M_A_ODT3 9,18

3,14,16,17,21,32 SMB_DATA_SB

3,14,16,17,21,32 SMB_CLK_SB

VDD_SPD_A

VDD_SPD_A 14

SA0_A2 1 10K_J 2 R220 0402

SA1_A2 1 10K_J 2 R221 0402

C122 0.1U_6.3V_K 0402_X5R

+0_9VRUN

C2368 4.7U_6.3V_K 0603_X5R

C2369 4.7U_6.3V_K 0603_X5R

1/1 changed from +1_8_S3_SUS to +0_9RUN

+1_8V_S3_SUS

C109 1U_10V_K 0402_X5R

C110 1U_10V_K 0402_X5R

C111 1U_10V_K 0402_X5R

C112 1U_10V_K 0402_X5R

+1_8V_S3_SUS

C114 0.1U_16V_Y 0402_Y5V

C115 0.1U_16V_Y 0402_Y5V

C116 0.1U_16V_Y 0402_Y5V

C117 0.1U_16V_Y 0402_Y5V

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: DDRII(CHANNEL A)

Size: A3 | Document Number: M841 DVT | Rev: 0.1

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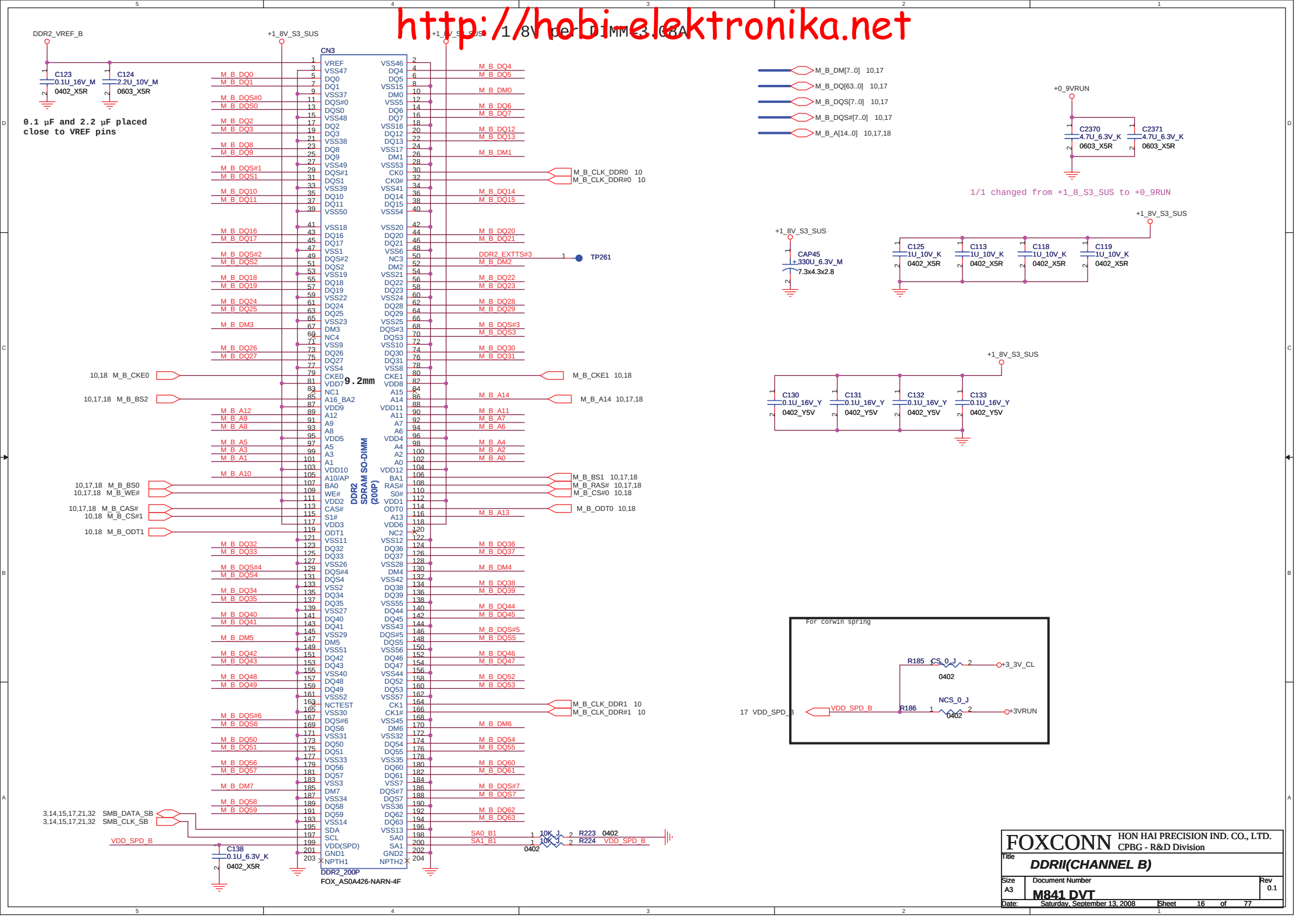

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
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DDR2_VREF_B

C139 0.1U_16V_M 0402_X5R

C140 2.2U_10V_M 0603_X5R

0.1 µF and 2.2 µF placed close to VREF pins

+1_8V_S3_SUS

+1_8V_S3_SUS

CN4

1	VREF	VSS46	2				
3	VSS47	DQ4	4	M_B_DQ4			
5	DQ0	DQ5	6	M_B_DQ5			
7	DQ1	VSS15	8				
9	VSS37	DM0	10	M_B_DM0			
11	DQS#0	VSS5	12				
13	DQS0	DQ6	14	M_B_DQ6			
15	VSS48	DQ7	16	M_B_DQ7			
17	DQ2	VSS16	18				
19	DQ3	DQ12	20	M_B_DQ12			
21	VSS38	DQ13	22	M_B_DQ13			
23	DQ8	VSS17	24				
25	DQ9	DM1	26	M_B_DM1			
27	VSS49	VSS53	28				
29	DQS#1	CK0	30	M_B_CLK_DDR3	10		
31	DQS1	CK0#	32	M_B_CLK_DDR#3	10		
33	VSS39	VSS41	34				
35	DQ10	DQ14	36	M_B_DQ14			
37	DQ11	DQ15	38	M_B_DQ15			
39	VSS50	VSS54	40				
41	VSS18	VSS20	42				
43	DQ16	DQ20	44	M_B_DQ20			
45	DQ17	DQ21	46	M_B_DQ21			
47	VSS1	VSS6	48				
49	DQS#2	NC3	50	DDR2_EXTTS#4	1	TP262	
51	DQS2	DM2	52	M_B_DM2			
53	VSS19	VSS21	54				
55	DQ18	DQ22	56	M_B_DQ22			
57	DQ19	DQ23	58	M_B_DQ23			
59	VSS22	VSS24	60				
61	DQ24	DQ28	62	M_B_DQ28			
63	DQ25	DQ29	64	M_B_DQ29			
65	VSS23	VSS25	66				
67	DM3	DQS#3	68	M_B_DQS#3			
69	NC4	DQS3	70	M_B_DQS3			
71	VSS9	VSS10	72				
73	DQ26	DQ30	74	M_B_DQ30			
75	DQ27	DQ31	76	M_B_DQ31			
77	VSS4	VSS8	78				
79	CKE0	CKE1	80	M_B_CKE3	10,18		
81	VDD7	VDD8	82				
83	NC1	A15	84				
85	A16_BA2	A14	86	M_B_A14	10,16,18		
87	VDD9	VDD11	88				
89	A12	A11	90	M_B_A11			
91	A9	A7	92	M_B_A7			
93	A8	A6	94	M_B_A6			
95	VDD5	VDD4	96				
97	A5	A4	98	M_B_A4			
99	A3	A2	100	M_B_A2			
101	A1	A0	102	M_B_A0			
103	VDD10	VDD12	104				
105	A10/AP	BA1	106	M_B_BS1	10,16,18		
107	BA0	RAS#	108	M_B_RAS#	10,16,18		
109	WE#	S0#	110	M_B_CS#2	10,18		
111	VDD2	VDD1	112				
113	CAS#	ODT0	114	M_B_ODT2	10,18		
115	S1#	A13	116	M_B_A13			
117	VDD3	VDD6	118				
119	ODT1	NC2	120				
121	VSS11	VSS12	122				
123	DQ32	DQ36	124	M_B_DQ36			
125	DQ33	DQ37	126	M_B_DQ37			
127	VSS26	VSS28	128				
129	DQS#4	DM4	130	M_B_DM4			
131	DQS4	VSS42	132				
133	VSS2	DQ38	134	M_B_DQ38			
135	DQ34	DQ39	136	M_B_DQ39			
137	DQ35	VSS55	138				
139	VSS27	DQ44	140	M_B_DQ44			
141	DQ40	DQ45	142	M_B_DQ45			
143	DQ41	VSS43	144				
145	VSS29	DQS#5	146	M_B_DQS#5			
147	DM5	DQS5	148	M_B_DQS5			
149	VSS51	VSS56	150				
151	DQ42	DQ46	152	M_B_DQ46			
153	DQ43	DQ47	154	M_B_DQ47			
155	VSS40	VSS44	156				
157	DQ48	DQ52	158	M_B_DQ52			
159	DQ49	DQ53	160	M_B_DQ53			
161	VSS52	VSS57	162				
163	NCTEST	CK1	164	M_B_CLK_DDR4	10		
165	VSS30	CK1#	166	M_B_CLK_DDR#4	10		
167	DQS#6	VSS45	168				
169	DQS6	DM6	170	M_B_DM6			
171	VSS31	VSS32	172				
173	DQ50	DQ54	174	M_B_DQ54			
175	DQ51	DQ55	176	M_B_DQ55			
177	VSS33	VSS35	178				
179	DQ56	DQ60	180	M_B_DQ60			
181	DQ57	DQ61	182	M_B_DQ61			
183	VSS3	VSS7	184				
185	DM7	DQS#7	186	M_B_DQS#7			
187	VSS34	DQS7	188	M_B_DQS7			
189	DQ58	VSS36	190				
191	DQ59	DQ62	192	M_B_DQ62			
193	VSS14	DQ63	194	M_B_DQ63			
195	SDA	VSS13	196				
197	SCL	SA0	198	SA0_B2	1 10K_J 2	R226 0402	VDD_SPD_B
199	VDD(SPD)	SA1	200	SA1_B2	1 10K_J 2	R227 0402	

SMDFIX1 SMDFIX2 NPTH1 NPTH2 201 202 203 204

5.2mm

DDR2_200P
FOX_AS0A426-N2RN-4F

M_B_DQ[0..7] M_B_DQ[8..15] M_B_DQ[16..23] M_B_DQ[24..31] M_B_DQ[32..39] M_B_DQ[40..47] M_B_DQ[48..55] M_B_DQ[56..63] M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7 M_B_DM[0..7] M_B_A[0..13] M_B_BS0 M_B_BS1 M_B_BS2 M_B_RAS# M_B_CAS# M_B_WE# M_B_CS#0 M_B_CS#1 M_B_CS#2 M_B_CS#3 M_B_ODT0 M_B_ODT1 M_B_ODT2 M_B_ODT3 M_B_CKE0 M_B_CKE1 M_B_CKE2 M_B_CKE3

10,18 M_B_CKE2

10,16,18 M_B_BS2

10,16,18 M_B_BS0
10,16,18 M_B_WE#

10,16,18 M_B_CAS#
10,18 M_B_CS#3

10,18 M_B_ODT3

3,14,15,16,21,32 SMB_DATA_SB
3,14,15,16,21,32 SMB_CLK_SB
16 VDD_SPD_B

C154 0.1U_6.3V_K 0402_X5R

M_B_DM[7..0] 10,16
M_B_DQ[63..0] 10,16
M_B_DQS[7..0] 10,16
M_B_DQS#[7..0] 10,16
M_B_A[14..0] 10,16,18

+0_9VRUN

C2372 4.7U_6.3V_K 0603_X5R

C2373 4.7U_6.3V_K 0603_X5R

1/1 changed from +1_8_S3_SUS to +0_9RUN

+1_8V_S3_SUS

Place these Caps near So-Dimm0.

C141 1U_10V_K 0402_X5R

C142 1U_10V_K 0402_X5R

C143 1U_10V_K 0402_X5R

C144 1U_10V_K 0402_X5R

+1_8V_S3_SUS

Place these Caps near So-Dimm0.

C146 0.1U_16V_Y 0402_Y5V

C147 0.1U_16V_Y 0402_Y5V

C148 0.1U_16V_Y 0402_Y5V

C149 0.1U_16V_Y 0402_Y5V

DDRDIMM_VREF +1_8V_S3_SUS

DDR2_VREF_B

(20 mil)

R109 NC_0_J 0402

R3691 1K_D 0402

R3692 820_D 0402

C2395 0.1U_16V_Y 0402_Y5V

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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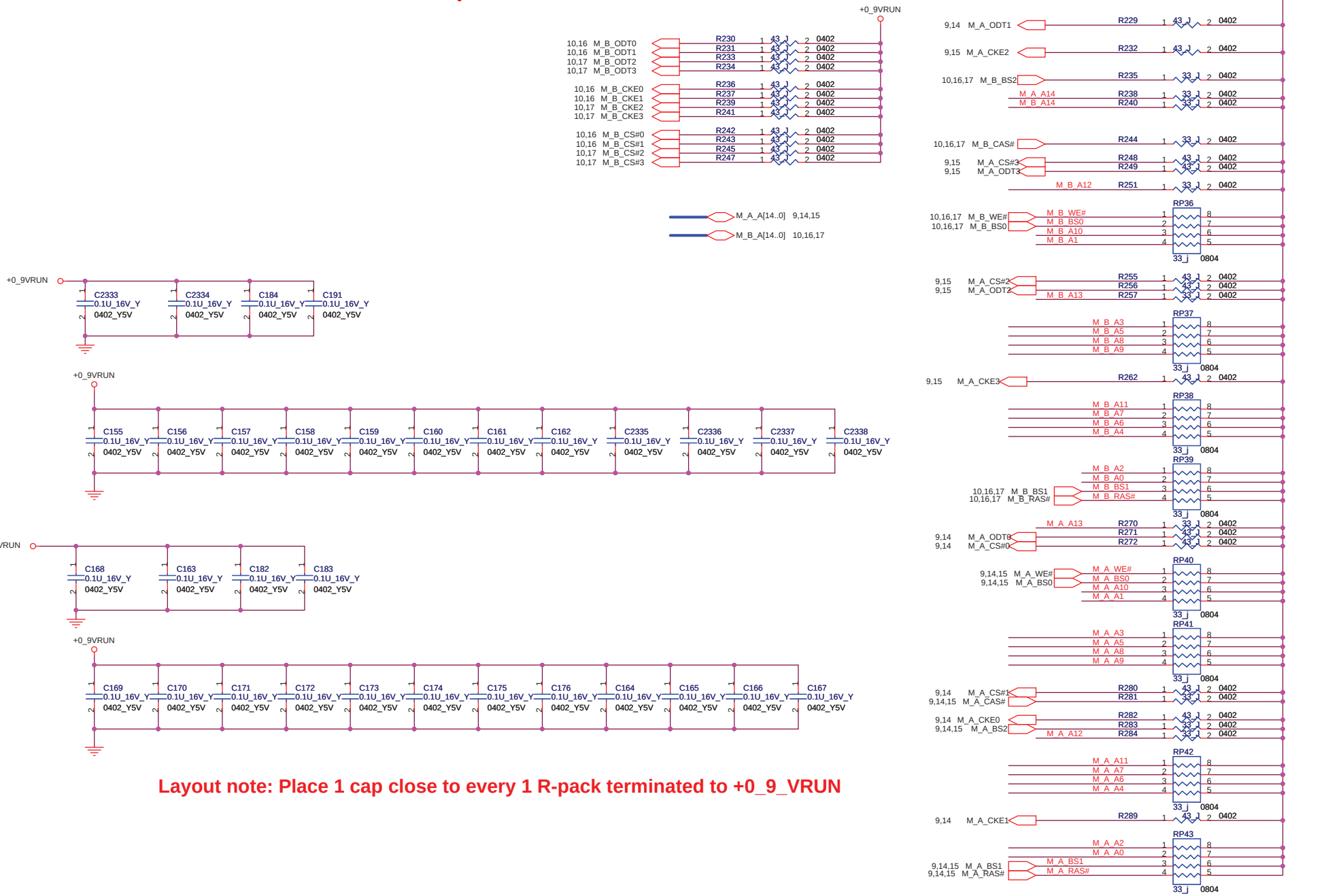

Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9_VRUN

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***DDRII Termination***	
Size A3	Document Number **M841 DVT**	Rev 0.1
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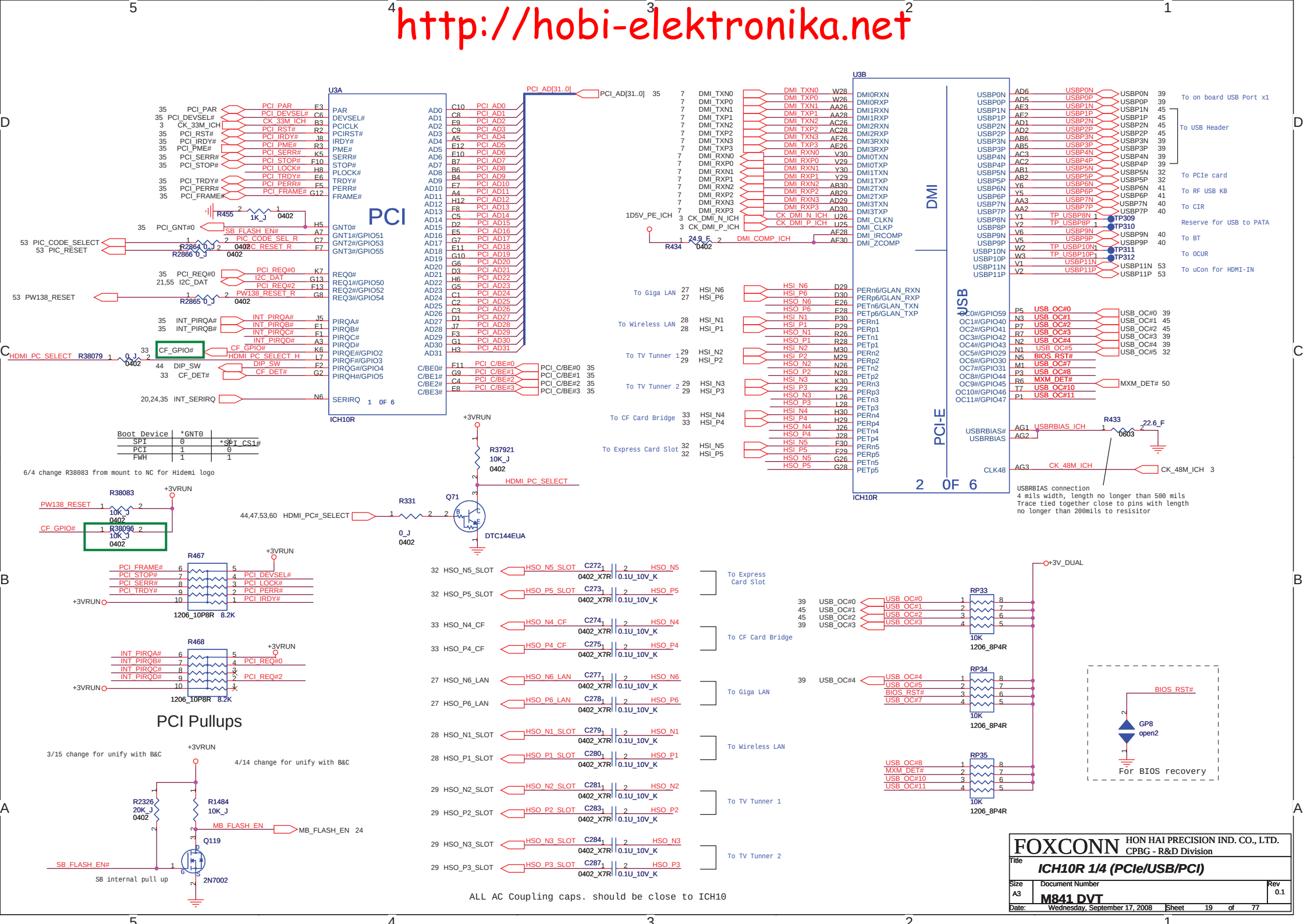

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	ICH10R 1/4 (PCIe/USB/PCI)
Size	A3
Document Number	M841 DVT
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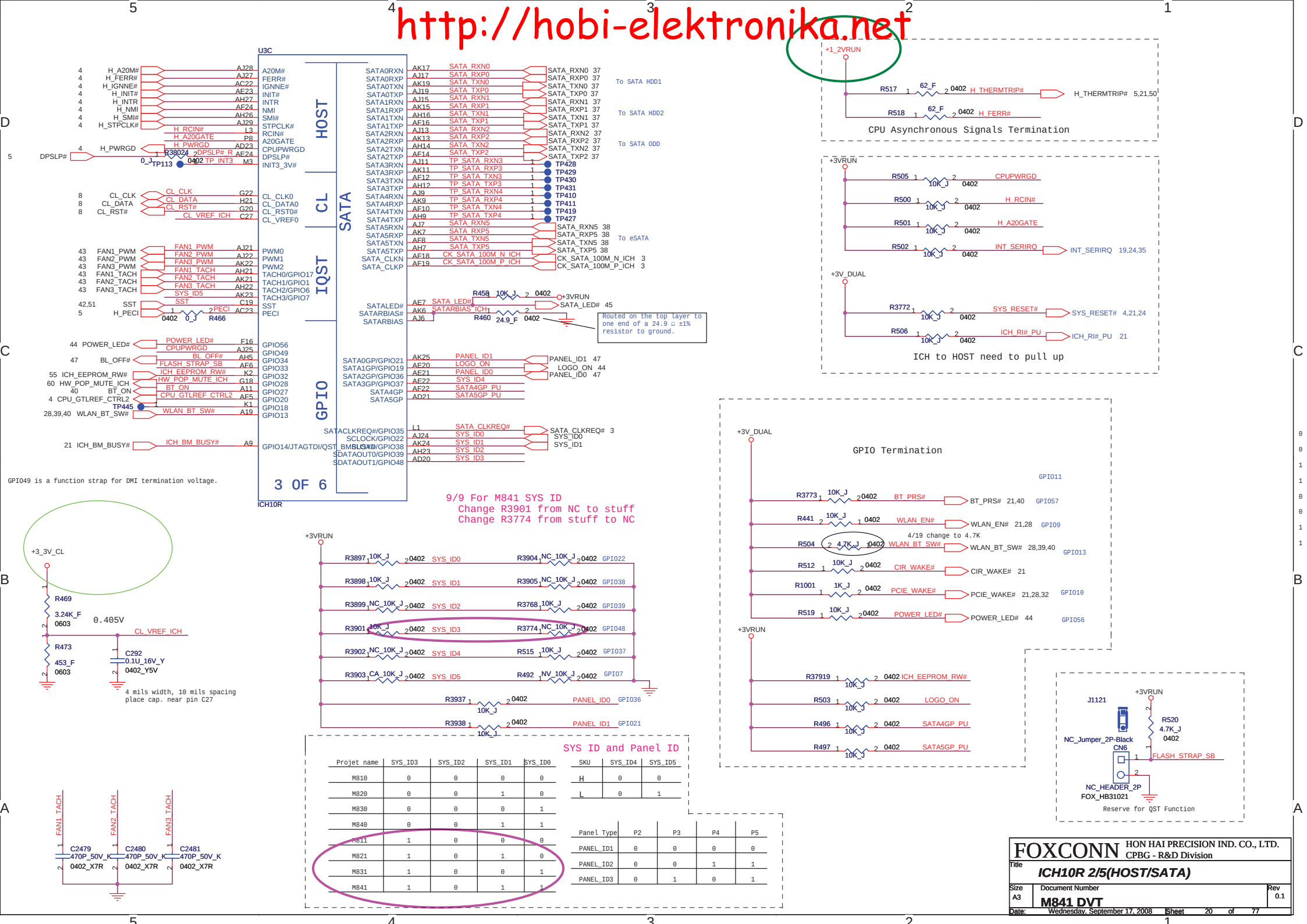

Projet name	SYS_ID3	SYS_ID2	SYS_ID1	SYS_ID0
M810	0	0	0	0
M820	0	0	1	0
M830	0	0	0	1
M840	0	0	1	1
M811	1	0	0	0
M821	1	0	1	0
M831	1	0	0	1
M841	1	0	1	1

SKU	SYS_ID4	SYS_ID5
H	0	0
L	0	1

Panel Type	P2	P3	P4	P5
PANEL_ID1	0	0	0	0
PANEL_ID2	0	0	1	1
PANEL_ID3	0	1	0	1

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ICH10R 2/5(HOST/SATA)

Size	Document Number	Rev
A3	M841 DVT	0.1

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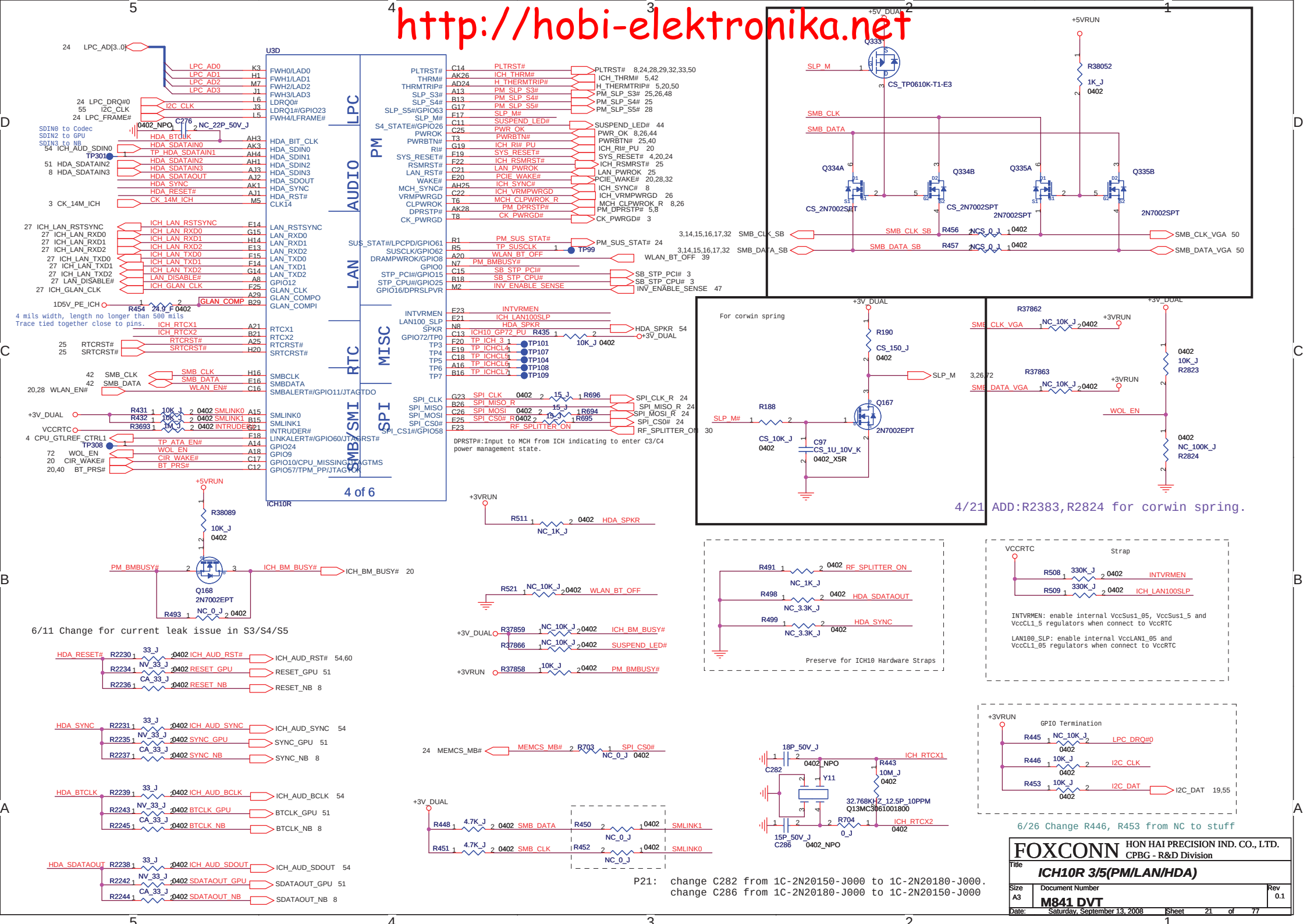

VccGLANPLL LRC Filter

+1_5VRUN — L41 1U_1206 TL321611-1R0K Rated at least 100mA — VCCGLANPLL — 23mA

C360 10U_10V_Y 0805_Y5V

C358 1U_10V_Y 0603_Y5V

Place LRC near pin A25

VccDMIPLL LRC Filter

+1_5VRUN — L38 1U_1206 TL321611-1R0K Rated at least 100mA — DMIPLL — R482 0_J 0402 — VCCDMIPLL — 23mA

C361 10U_10V_Y 0805_Y5V

C475 0.01U_25V_K 0603_X7R

Place LRC near pin T30

PCI-E (VCC1_5_B) Filter

+1_5VRUN — L75 1U_1210 EBLS3225-1R0M 1A — 1D5V_PE_ICH

C384 22U_6.3V_M 0805_X5R

C337 22U_6.3V_M 0805_X5R

C359 2.2U_10V_Y 0603_Y5V

C333 4.7U_6.3V_K 0603_X5R

Place C384, C337, C359 near AE30

Place C333 near B30

VccSATAPLL LC Filter

+1_5VRUN — L76 10UH_0.1A_1.15R TW201212-100M — SATAPLL — R486 0_J 0402 — VCCSATAPLL — 47mA

C1854 10U_10V_Y 0805_Y5V

C1855 1U_10V_Y 0603_Y5V

Place LC near pin AK20

+1_5VRUN

CAP51 330U_2V_T EEFSX0D331ER

C2556 4.7U_6.3V_K 0603_X5R

C2528 4.7U_6.3V_K 0603_X5R

C2529 0.1U_16V_Y 0402_Y5V

C2530 0.1U_16V_Y 0402_Y5V

VCC_CL1_05 — C302 0.1U_16V_Y 0402_Y5V — place near A23

VCCLAN1_05 — C526 1U_10V_Y 0603_Y5V — C297 1U_6.3V_K 0402_X5R — place near A10 or B10

ICH10R

2mA	REF5V_SUS	A6	V5REF
		AF1	V5REF_Sus
VCC_HDA	VCC_CL1_5	A26	VccCL1_5
	VCC_CL1_05	A23	VccCL1_1
32mA	VCCSUSHDA	AC9	VccSusHDA
32mA	VCC_HDA	AC10	VccHDA
11mA		AK5	VccUSBPLL
VCCSATAPLL		AK20	VccSATAPLL
	VCCDMIPLL	T30	VccDMIPLL
	VCCGLANPLL	A28	VccGLANPLL
	VCCLAN1_05 For LAN IO	B10	VccLAN1_1_2
		A10	VccLAN1_1_1
		C30	VccGLAN1_5_4
80mA	1D5V_PE_ICH	C29	VccGLAN1_5_3
		C28	VccGLAN1_5_2
		B30	VccGLAN1_5_1

1D5V_PE_ICH — 646mA

AA23	Vcc1_5_B_1
AA24	Vcc1_5_B_2
AA25	Vcc1_5_B_3
AB24	Vcc1_5_B_4
AB25	Vcc1_5_B_5
AC25	Vcc1_5_B_6
AD25	Vcc1_5_B_7
AD26	Vcc1_5_B_8
AD28	Vcc1_5_B_9
AE28	Vcc1_5_B_10
AE29	Vcc1_5_B_11
AE30	Vcc1_5_B_12
J24	Vcc1_5_B_13
J25	Vcc1_5_B_14
K23	Vcc1_5_B_15
K24	Vcc1_5_B_16
K25	Vcc1_5_B_17
L24	Vcc1_5_B_18
L25	Vcc1_5_B_19
M23	Vcc1_5_B_20
M24	Vcc1_5_B_21
M25	Vcc1_5_B_22
N24	Vcc1_5_B_23
N25	Vcc1_5_B_24
P23	Vcc1_5_B_25
P24	Vcc1_5_B_26
P25	Vcc1_5_B_27
R24	Vcc1_5_B_28
R25	Vcc1_5_B_29
T23	Vcc1_5_B_30
T24	Vcc1_5_B_31
T25	Vcc1_5_B_32
T26	Vcc1_5_B_33
T28	Vcc1_5_B_34
U24	Vcc1_5_B_35
U28	Vcc1_5_B_36
U29	Vcc1_5_B_37
U30	Vcc1_5_B_38
V23	Vcc1_5_B_39
V24	Vcc1_5_B_40
V25	Vcc1_5_B_41
W24	Vcc1_5_B_42
W25	Vcc1_5_B_43
Y23	Vcc1_5_B_44
Y24	Vcc1_5_B_45
Y25	Vcc1_5_B_46

+1_1VRUN — 50mA — AG29 VccDMI_1 — AG30 VccDMI_2

+1_5VRUN — 1644mA

H10	Vcc1_5_A_30
H11	Vcc1_5_A_31
AC11	Vcc1_5_A_6
AB23	Vcc1_5_A_3
AC18	Vcc1_5_A_12
AC20	Vcc1_5_A_13
AC13	Vcc1_5_A_7
AD11	Vcc1_5_A_14
AD12	Vcc1_5_A_15
AD13	Vcc1_5_A_16
AE11	Vcc1_5_A_18
AF11	Vcc1_5_A_20
AH10	Vcc1_5_A_22
AH11	Vcc1_5_A_23
AJ10	Vcc1_5_A_26
AK10	Vcc1_5_A_28
AC17	Vcc1_5_A_11
AD17	Vcc1_5_A_17
AE17	Vcc1_5_A_19
AF17	Vcc1_5_A_21
AH17	Vcc1_5_A_24
AH18	Vcc1_5_A_25
AJ18	Vcc1_5_A_27
AK18	Vcc1_5_A_29

5 OF 6

	VccCL3_3_1	B23	
	VccCL3_3_2	C23	

place near C23 or B23 — C295 0.1U_10V_K 0402_X5R

+1_5VRUN — 1644mA

	Vcc1_5_A_1	AA7	
	Vcc1_5_A_2	AA8	
	Vcc1_5_A_4	AB7	
	Vcc1_5_A_5	AB8	
	Vcc1_5_A_32	T1	
	Vcc1_5_A_8	AC14	
	Vcc1_5_A_9	AC15	
	Vcc1_5_A_10	AC16	

+1_1VRUN — 1634mA

	Vcc1_1_1	A24	
	Vcc1_1_2	B24	
	Vcc1_1_3	C24	
	Vcc1_1_4	F24	
	Vcc1_1_5	F24	
	Vcc1_1_6	G24	
	Vcc1_1_7	H23	
	Vcc1_1_8	H24	
	Vcc1_1_9	J23	
	Vcc1_1_10	M12	
	Vcc1_1_11	M13	
	Vcc1_1_12	M15	
	Vcc1_1_13	M17	
	Vcc1_1_14	M18	
	Vcc1_1_15	M19	
	Vcc1_1_16	N12	
	Vcc1_1_17	N19	
	Vcc1_1_18	R12	
	Vcc1_1_19	R19	
	Vcc1_1_20	U12	
	Vcc1_1_21	U19	
	Vcc1_1_22	V12	
	Vcc1_1_23	V19	
	Vcc1_1_24	W12	
	Vcc1_1_25	W13	
	Vcc1_1_26	W15	
	Vcc1_1_27	W17	
	Vcc1_1_28	W18	
	Vcc1_1_29	W19	

+1_2VRUN — 2mA

	V_CPU_IO_1	AH28	
	V_CPU_IO_2	AJ30	

+3VRUN — 1mA

	VccGLAN3_3	A27	For LAN Core
	VccLAN3_3_1	A12	
	VccLAN3_3_2	B12	

+3_3V_CL — 78mA

+3VRUN — 308mA

	Vcc3_3_6	AH24	
	Vcc3_3_5	AF21	
	Vcc3_3_3	AC21	
	Vcc3_3_2	AC19	
	Vcc3_3_4	AD10	
	Vcc3_3_7	AH30	
	Vcc3_3_8	AK4	
	Vcc3_3_1	A2	
	Vcc3_3_9	B1	
	Vcc3_3_10	B9	
	Vcc3_3_11	G11	
	Vcc3_3_12	G3	
	Vcc3_3_13	H7	
	Vcc3_3_14	J2	
	Vcc3_3_15	K8	
	Vcc3_3_16	L8	

+3V_DUAL — 212mA

	VccSus3_3_2	AF2	
	VccSus3_3_7	U1	
	VccSus3_3_8	U2	
	VccSus3_3_9	U3	
	VccSus3_3_10	U5	
	VccSus3_3_11	U6	
	VccSus3_3_12	U7	
	VccSus3_3_13	U8	
	VccSus3_3_14	V8	
	VccSus3_3_15	W7	
	VccSus3_3_16	W8	
	VccSus3_3_17	Y8	
	VccSus3_3_1	A17	
	VccSus3_3_3	B20	
	VccSus3_3_4	C20	
	VccSus3_3_5	F17	
	VccSus3_3_6	H15	

VCCRTC — VccRTC — A22

	VccSus1_1_1	AC7	1D05V_ICH_SB
	VccSus1_1_2	H17	
	VccSus1_5_2	H18	1D5V_ICH_SB
	VccSus1_5_1	AD8	

C310 0.1U_16V_K 0402_X7R

C311 0.1U_16V_Y 0402_Y5V

Near AC7 or H17

Near H18 or AD8

V5REF_SUS/+3V_DUAL Power Sequencing

+3V_DUAL — +3V_DUAL — R483 10_J 0402 — D39 CH035H-40PT — REF5V_SUS

C1853 0.1U_16V_Y 0402_Y5V — place C1853 near pin AF1

V5REF / +3VRUN Power Sequencing

+5VRUN — +3VRUN — R481 10_J 0402 — D38 CH035H-40PT — REF5V

C362 0.1U_16V_Y 0402_Y5V — place C362 near pin A6

VCC_HDA Decoupling

VCC_HDA — R484 NV_0_J 0402 — +3VRUN — +1_5VRUN — VCC_HDA — R485 CA_0_J 0402 BACK — BACK

C332 0.1U_25V_Y 0603_Y5V — place C332 near pin AC10

+3V_DUAL — R494 NV_0_J 0402 — R488 CA_237_F 0402 — VCCSUSHDA — R490 CA_200_F 0402

C336 0.1U_25V_Y 0603_Y5V — place C336 near pin AC9

+1_1VRUN — C177 0.022U_25V_K 0402_X7R — C178 0.1U_16V_Y 0402_Y5V — Place 0.022U_25V_K — place near ICH10

VCC_CL1_5 — C301 0.1U_16V_Y 0402_Y5V — C477 1U_10V_Y 0603_Y5V — C477 can be delete — place near A26

+1_2VRUN — Placed near AH28 and AJ30 — C179 0.1U_16V_Y 0402_Y5V — C180 0.1U_16V_Y 0402_Y5V — C181 4.7U_6.3V_K 0603_X5R

+3VRUN — C328 0.1U_16V_K 0402_X7R — Near B1

PCI decoup caps

+1_5VRUN — 1644mA — +3VRUN

C312 1U_10V_Y 0603_Y5V — C313 1U_10V_Y 0603_Y5V — C321 0.1U_16V_K 0402_X7R

Near AK18,AK10 — Near AK4

SATA decoupling caps.

+3V_DUAL — VCC_HDA — C314 0.1U_16V_K 0402_X7R — C315 0.1U_16V_K 0402_X7R — Near AC9 and AC10

Audio decoupling caps

+3VRUN — C335 0.1U_16V_Y 0402_Y5V — Near AE20

PCI-E decoup caps.

+1_1VRUN — C318 0.1U_16V_K 0402_X7R — C319 0.1U_16V_K 0402_X7R — C320 4.7U_6.3V_K 0805_X5R — Near AH28 and AJ30

CPU decoupling caps.

+3V_DUAL — C327 0.1U_16V_K 0402_X7R — Near A12

LAN decoupling

+3V_DUAL — +1_5VRUN — C322 0.1U_16V_K 0402_X7R — C323 0.022U_16V_M 0402_X7R — C316 0.1U_16V_K 0402_X7R — C317 0.1U_16V_K 0402_X7R

C322 near AF2 — C323 near U1 — C316 near T1 — C317 near AK5

USB decoupling caps.

VCCRTC — C324 0.1U_16V_K 0402_X7R — C325 0.1U_16V_K 0402_X7R — C326 1U_10V_K 0402_X5R — Near ball A22

RTC decoupling caps.

+1_1VRUN — C334 22U_6.3V_K 1206_X5R — Near AG30

DMI decoupling

+1_1VRUN — C330 0.022U_16V_K 0402_X7R — C331 0.1U_10V_K 0402_X7R — Near A24

ICH Core decoup caps.

FOXCONN — HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division

Title: ICH10R 4/5(Power)

Size: A3 — Document Number: M841 DVT — Rev: 0.1

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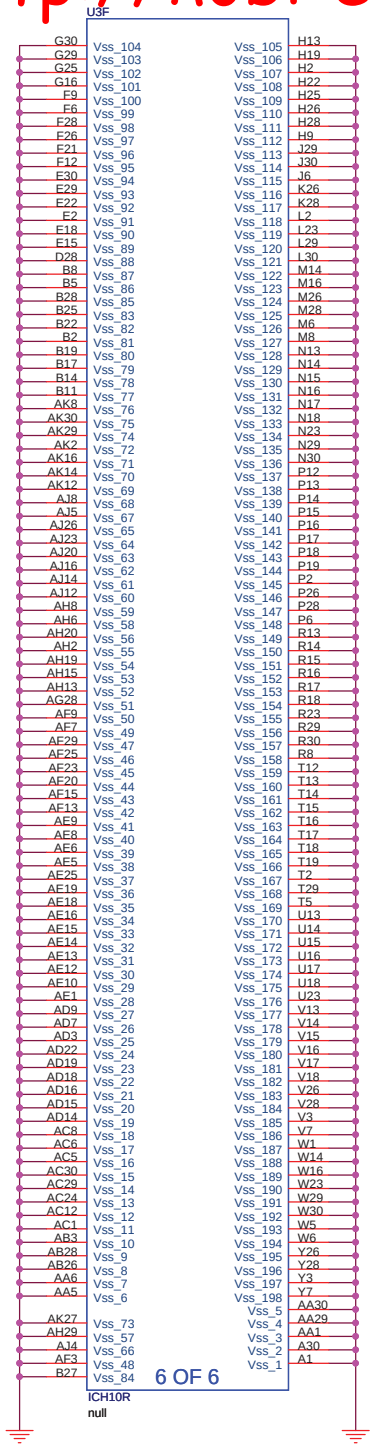

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*ICH10R 5/5(Ground)*	
Size A3	Document Number **M841 DVT**	Rev 0.1
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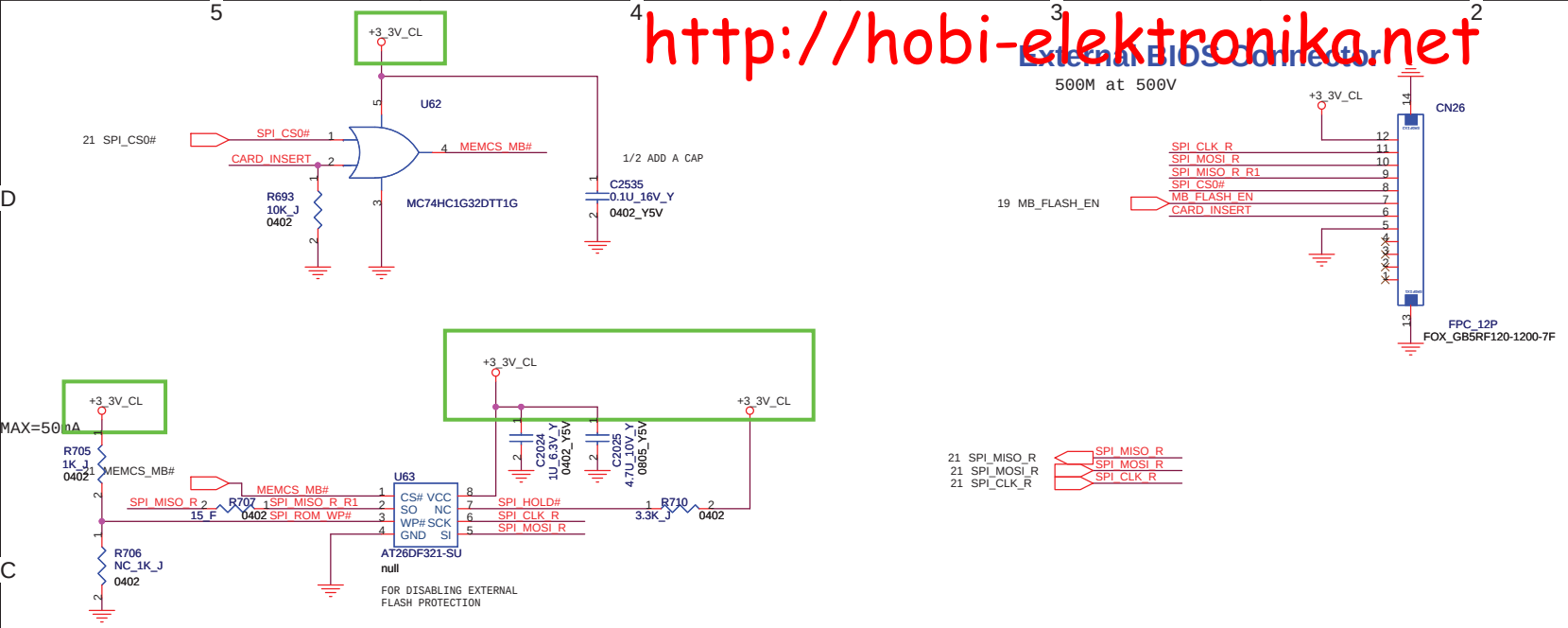


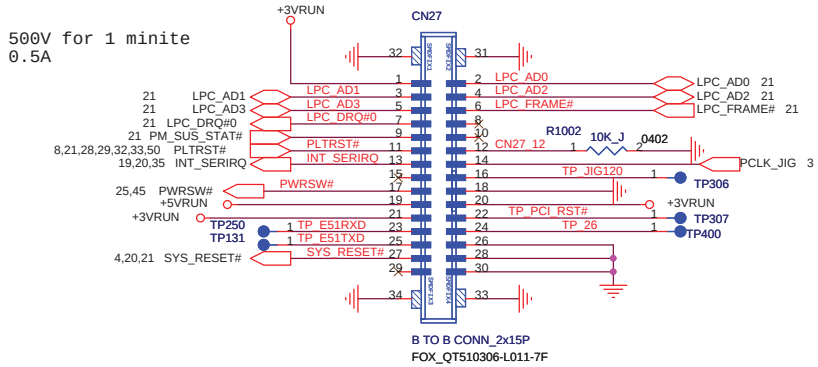
External BIOS Connector

500M at 500V

SPI Interface BIOS

JIG-120 Connector

500V for 1 minite
0.5A



ID_LPC_PCI#:Detect 80 port by LPC or PCI bus.
(Debug card did not use this signal right now)
PCLK_JIG
PCLK_FWH
PCI_RST#
SYS_RESET#General SMI# from JIG-120
(Connect through a switch to GND on debug card)
CARD_INSERT
PWRSW#
PLTRST# RESSET外設
PM_SUS_STAT# LPC power down
LPC_DRQ#0
MB_EXT_SEL

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
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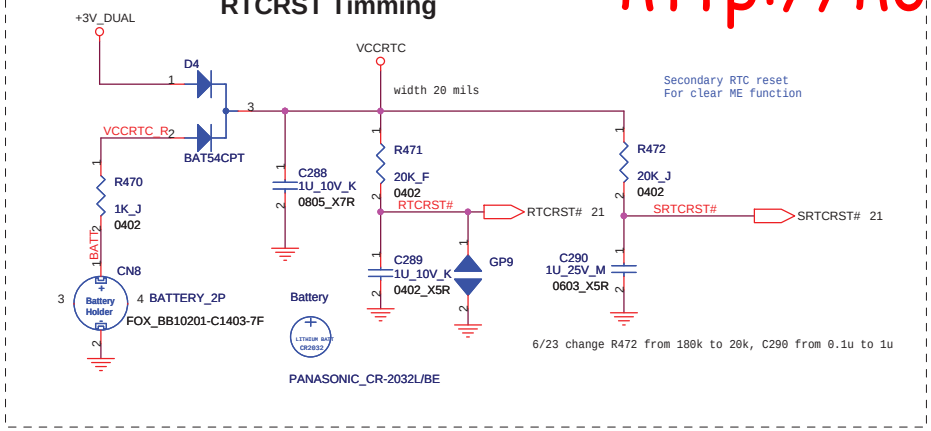
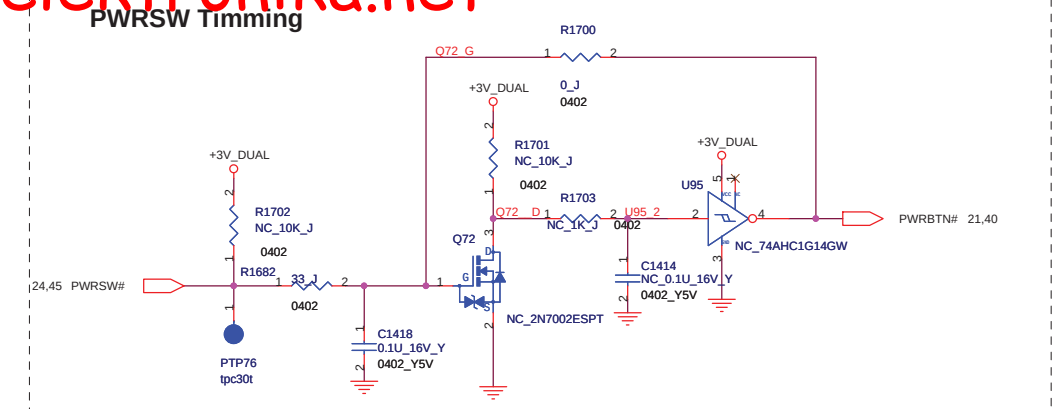
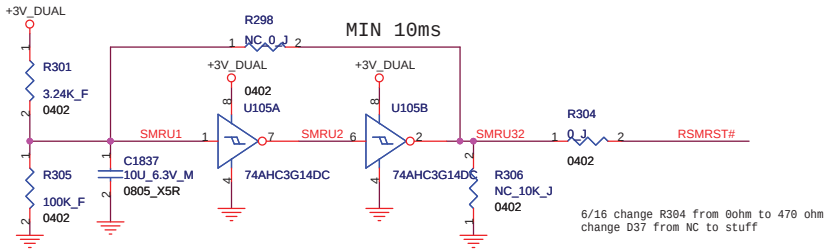
RTCRST Timming



PWRSW Timming

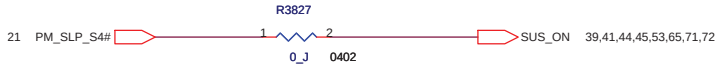


RSMRST Timming



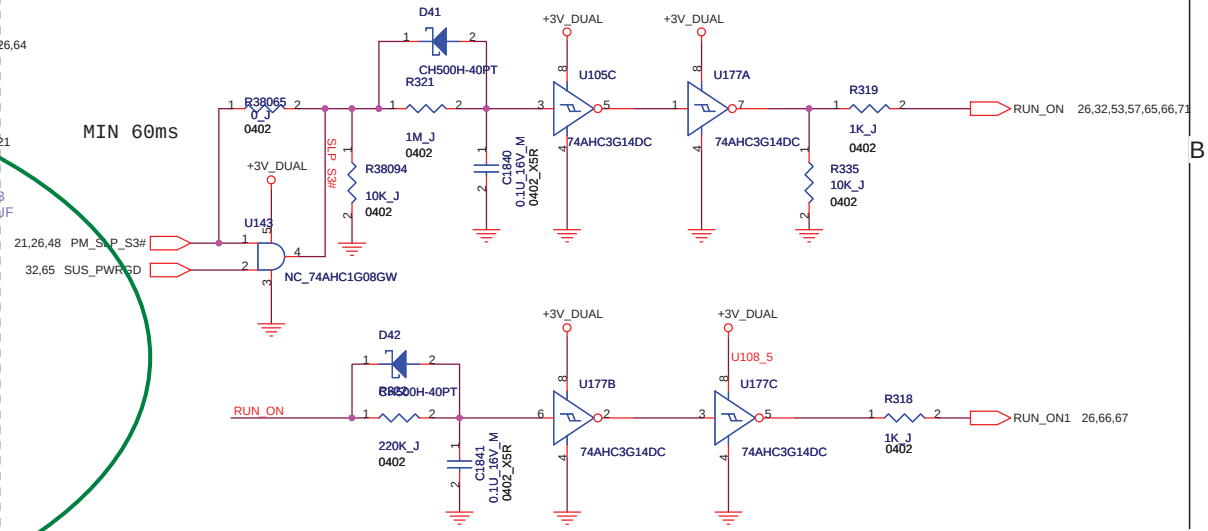
RSMRET# falling edge must transition to 0.8 V
or less before +3V_DUAL drops to 2.1V

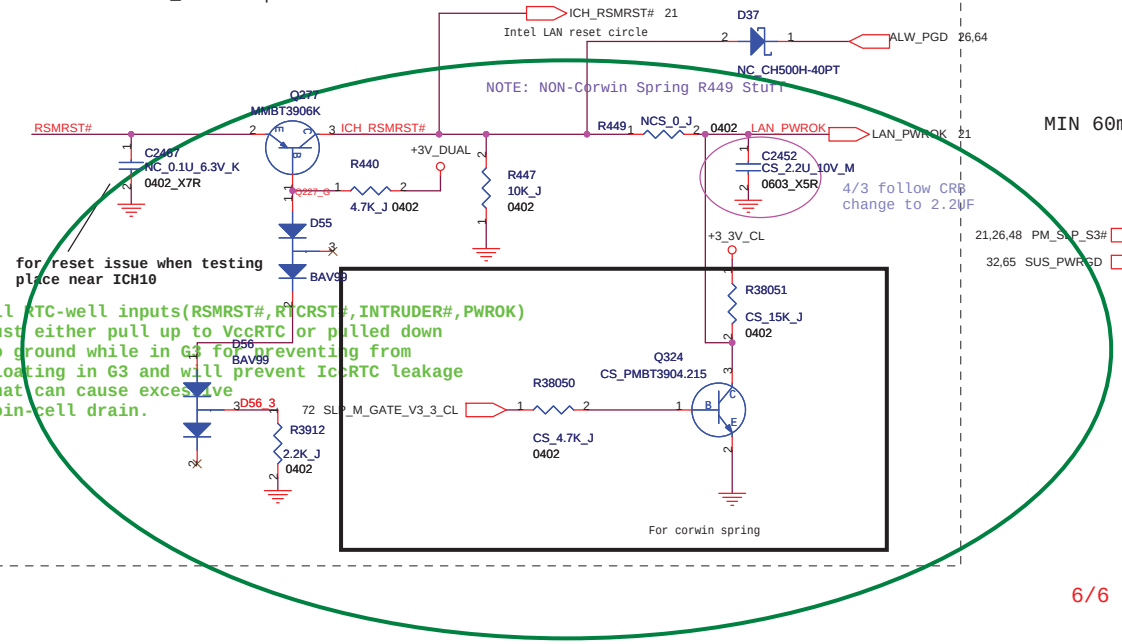
SLP_S4#



P25: Change R38094 form NC to 1R-0000103-J200

SLP_S3# --> RUN_ON





All RTC-well inputs(RSMRST#,RTCRST#,INTRUDER#,PWROK)
must either pull up to VccRTC or pulled down
to ground while in G3 for preventing from
floating in G3 and will prevent IccRTC leakage
that can cause excessive
coin-cell drain.

6/6 unify sequence circuit with B&C

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VRMPWRGD

4/14 DVT unify with B,C

+3VRUN — R297 NC_0_J 0402 — +3V_DUAL — R300 0_J 0402

R323 10K_J 0402 — MIN 10ms — R324 10K_J 0402 — D40 CH500H-40PT

VCC3_3P3STBY_PIN2 — SLP_S3_VR_READY_PIN5

68 VRM_PWRGD — R329 10K_J 0402 — Q171B CH3904SPT — C1843 NC_0.1U_16V_M 0402_X5R — Q171A CH3904SPT

R307 100K_J 0402 — R308 NC_100K_J 0402 — C1839 0.1U_16V_M 0402_X5R

U115 74AHC1G14GW — U107 74AHC1G14GW

R38030 1K_J 0402 — VRM_PWRGD_U — R38059 100K_J 0402

R330 0 0402 — ICH_VRMPWRGD 21

NCS_0_J R327 0402

6/6 unify sequence circuit with B&C

03/11 Change this circuit to keep same with B/C

+3V_DUAL — R38031 2.2K_J 0402 — Q314_3 — Q314 PMBT3904.215

+1_2VRUN — R38032 1K_J 0402 — Q315_3 — Q315 2N7002EPT

VRM_PWRGD_U — R332 10K_J 0402 — Q314_1

Q315_3 — R328 0_J 0402 — VRMPWRGD_CPU 5

+3_3V_CL — R38048 CS_1K_J 0402 — C2642 CS_1U_10V_Y 0603_Y5V

+5V_DUAL — R38047 CS_5.6K_J 0402

+1_1V_CL — C1438 CS_4.7U_6.3V_K 0603_X5R — C1439 CS_1U_6.3V_Y 0402_Y5V

R1647 CS_10K_J 0402 — Q332A — Q332B CS_CH3904SPT null — CS_CH3904SPT null

R333 CS_0_J 0402 — MCH_CLPWROK_R 8,21

Q323 CS_PMBT3904.215 — R38049 CS_1K_J 0402 — SLP_M 3,21,72

For corwin spring

RUN_PWRGD -->VID_GD

35,52,53,66 RUN_PWRGD — R296 0_J 0402 — VID_GD 68

VRMPWRGD --> PWR_OK

1_1VRUN TO PWROK >99mS

+3V_DUAL — R302 1M_J 0402 D36 — CH500H-40PT

ICH_VRMPWRGD — IVP1 — U106A — IVP2 — U106B — IVP3 — R303 1K_F 0402 — PWR_OK 8,21,44

C1838 0.22U_10V_M 0402_X5R — 74AHC3G14DC — R334 10K_J 0402

74AHC3G14DC 02/18:Delete this part because add discharge circuit

+3V_DUAL — U106C 74AHC3G14DC

SHUTDOWN Timming

RUN_ON 25,32,53,57,65,66,71 — Q341A — PWR_DWN_H — 2N7002SPT

VRM_PWRGD_U — Q305B — PWR_DWN_H — 2N7002SPT

VID_GD — Q305A — PWR_DWN_H — 2N7002SPT

RUN_ON1 25,66,67 — Q341B — PWR_DWN_H — 2N7002SPT

PWR_OK — Q124B — PWR_DWN_H — 2N7002SPT

+3V_DUAL — R1646 10K_J 0402 — PWR_DWN_H — Q124A — 2N7002SPT

5/16 change RUN_PWRGD to ALW_PGD

21,25,48 PM_SLP_S3# — U145 74AHC1G08GW

25,64 ALW_PGD

04/18:unify dischange circuit

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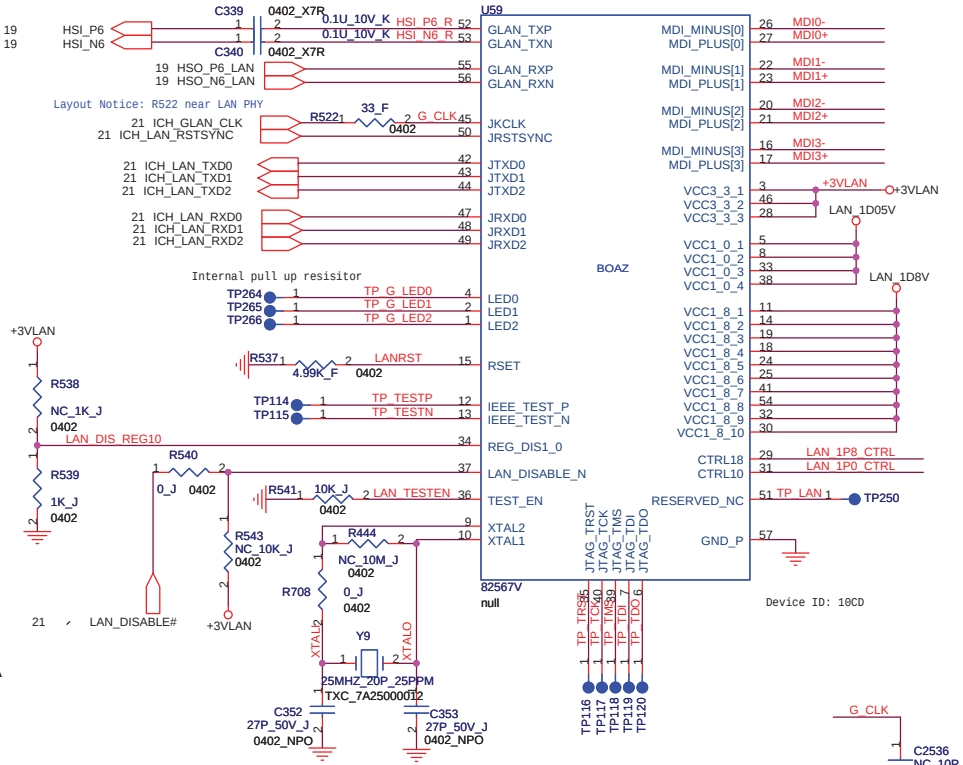
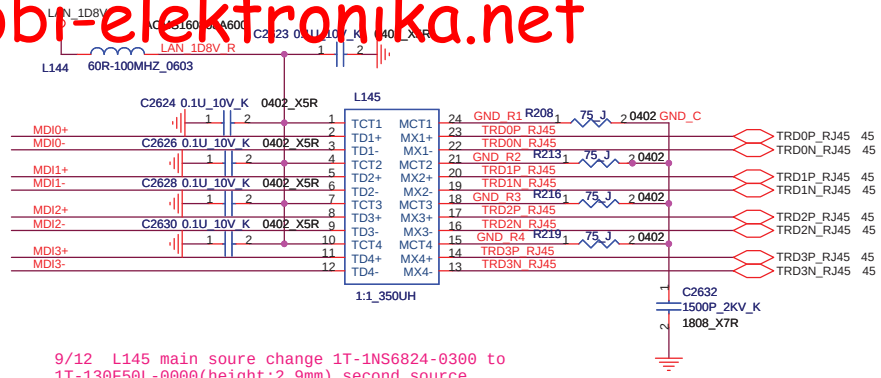
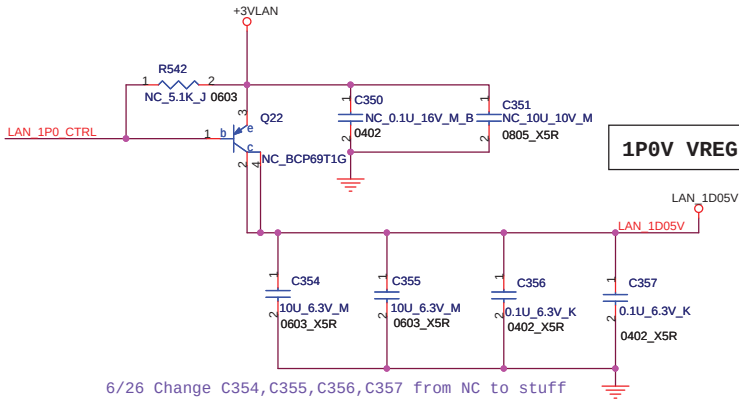
In 1000 Mb/s mode, JKCLK frequency is 62.5 MHz.
In 100 Mb/s mode, JKCLK frequency is 50 MHz.
In 10 Mb/s mode, JKCLK frequency is 5 MHz.
In power down mode, JKCLK frequency is 0 MHz.



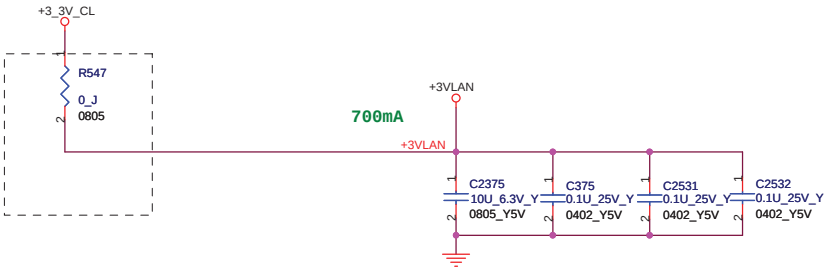


9/12 L145 main soure change 1T-1NS6824-0300 to 1T-130F50L-0000(height:2.9mm),second source 1T-130F500-0000(height:2.5mm)

Pls split a ground plane beneath the magnetics module(L61).



1P0V VREG (Analog Rail)

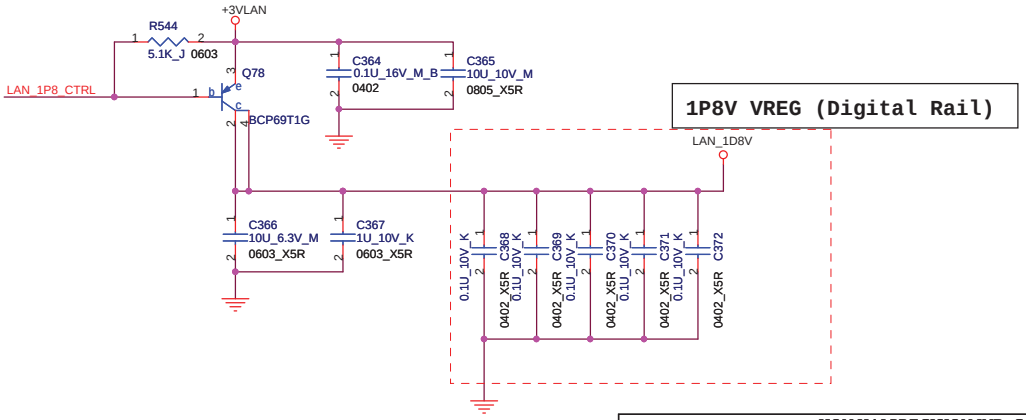


Place near pin3, pin46 and pin28.

0103
Add 10p to follow EMI suggest

6/26 Change C354,C355,C356,C357 from NC to stuff

Close to chip



1P8V VREG (Digital Rail)

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
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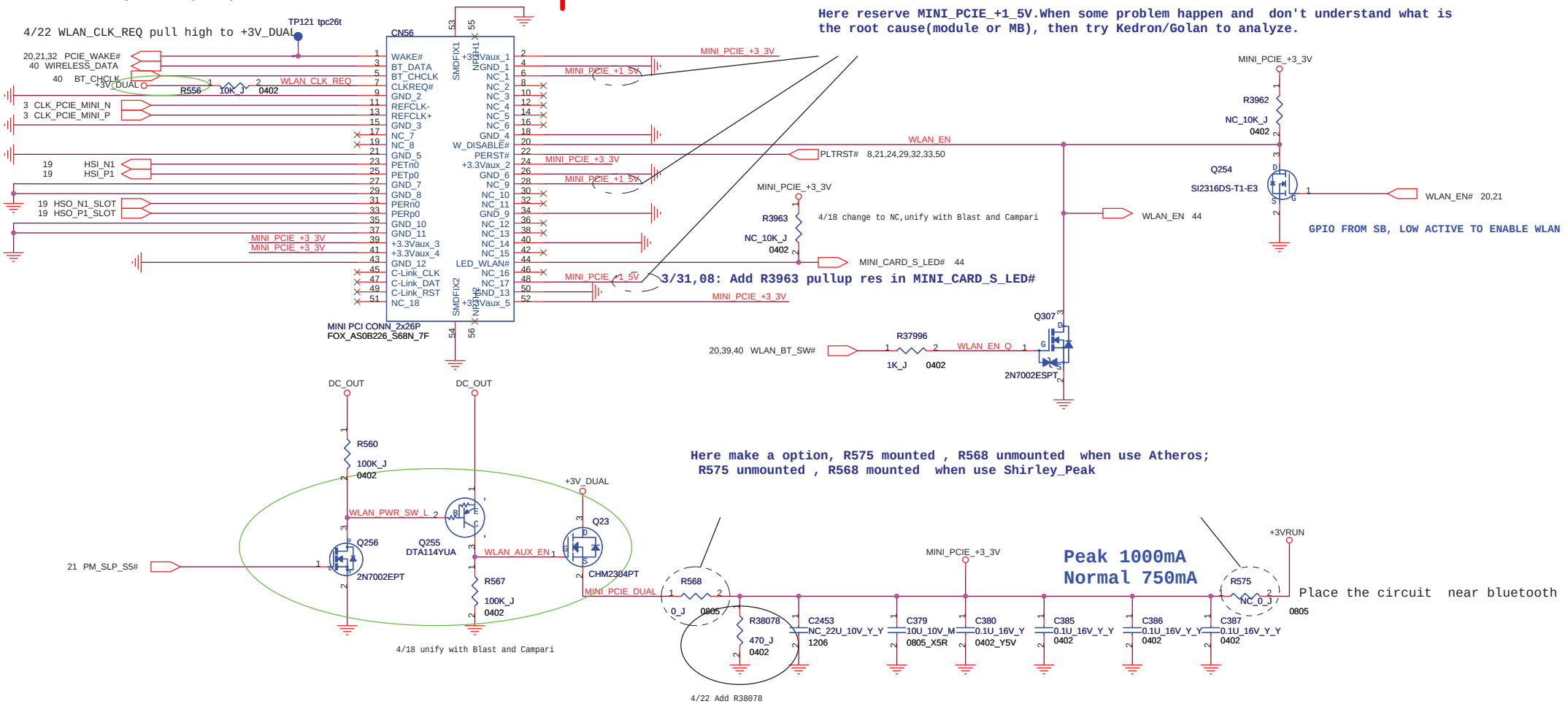
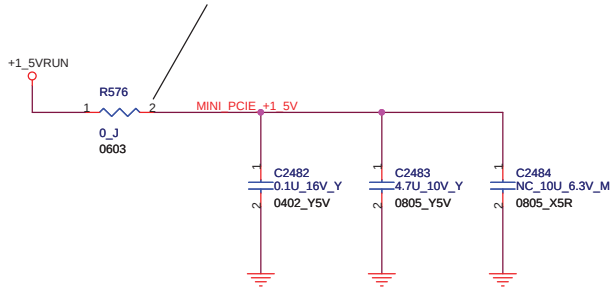
3/31,08: Change R556 pullup res from NC_0ohm to 10K

4/22 WLAN_CLK_REQ pull high to +3V_DUAL

Here reserve MINI_PCIE_+1_5V.When some problem happen and don't understand what is the root cause(module or MB), then try Kedron/Golan to analyze.



Here reserve MINI_PCIE_+1_5V.When some problem happen and don't understand what is the root cause(module or MB), then try Kedron/Golan to analyze.



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCIe WLAN		
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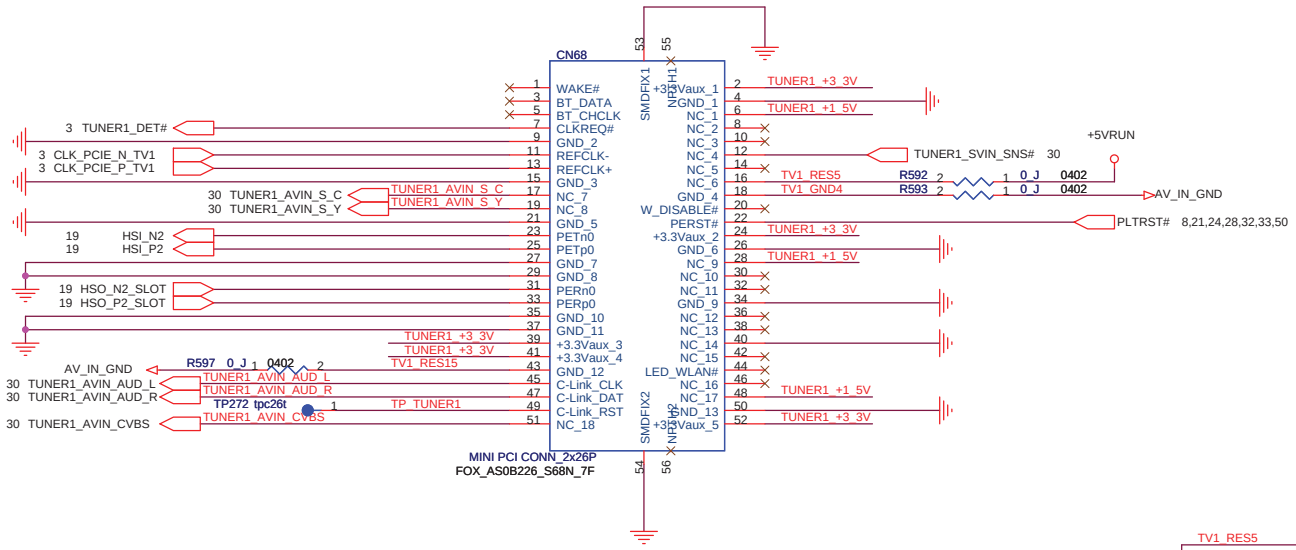
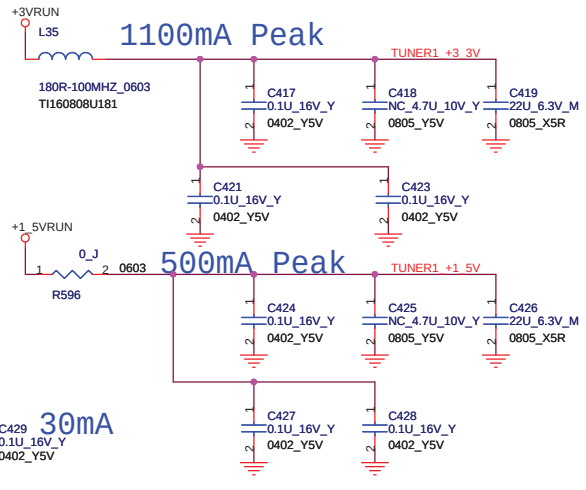
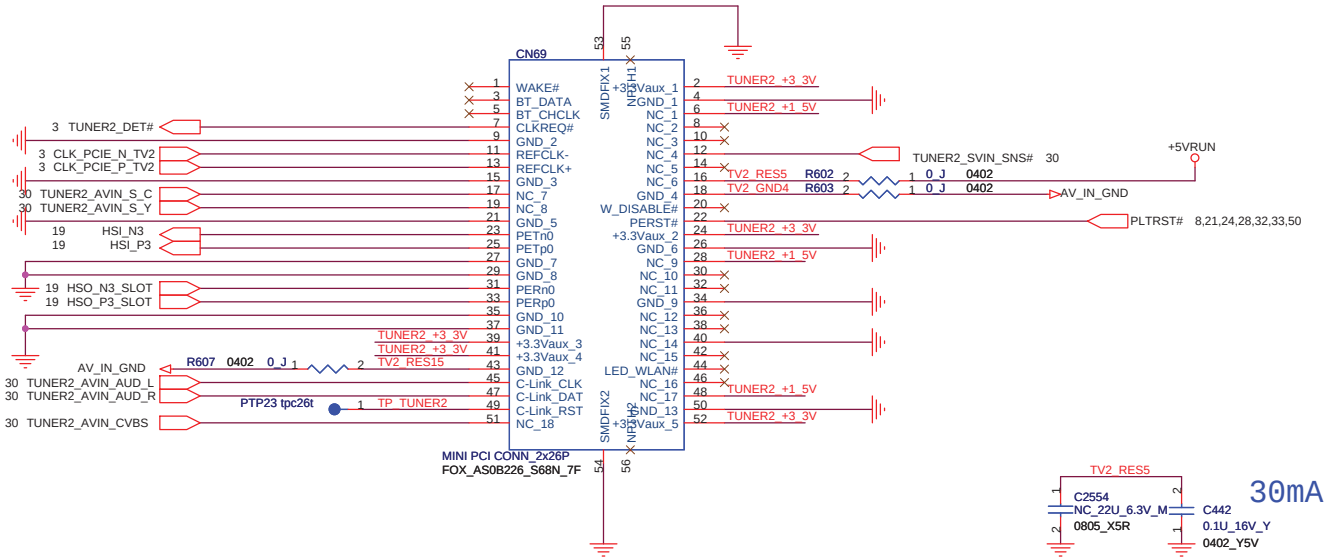
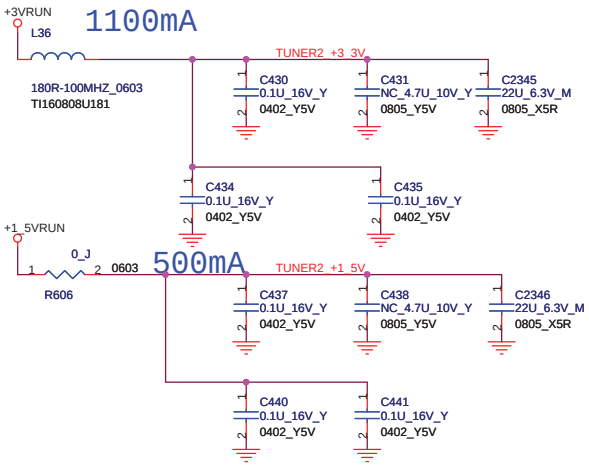
Mini-PCIE TUNER1 connector

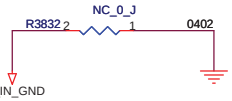




Mini-PCIE TUNER2 connector







FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: TV-TUNER1 /TV-TUNER1

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9/12 Change this circuit from NC to stuff for EU
TV tuner evaluation

AV_IN/SVIDEO IN/RF Splitter Power

29 TUNER1_AVIN_S_C — TUNER1_AVIN_S_C — R610 — 0_J — 0402 — SVIN_C
29 TUNER2_AVIN_S_C — TUNER2_AVIN_S_C — R611 — NC_0_J — 0402
29 TUNER1_AVIN_S_Y — TUNER1_AVIN_S_Y — R612 — 0_J — 0402 — SVIN_Y
29 TUNER2_AVIN_S_Y — TUNER2_AVIN_S_Y — R613 — NC_0_J — 0402
29 TUNER1_AVIN_AUD_L — TUNER1_AVIN_AUD_L — R615 — 0_J — 0402 — AUDIO_IN_L
29 TUNER2_AVIN_AUD_L — TUNER2_AVIN_AUD_L — R616 — NC_0_J — 0402
29 TUNER1_AVIN_AUD_R — TUNER1_AVIN_AUD_R — R618 — 0_J — 0402 — AUDIO_IN_R
29 TUNER2_AVIN_AUD_R — TUNER2_AVIN_AUD_R — R620 — NC_0_J — 0402
29 TUNER1_AVIN_CVBS — TUNER1_AVIN_CVBS — R621 — 0_J — 0402 — VIDEO_COMP
29 TUNER2_AVIN_CVBS — TUNER2_AVIN_CVBS — R622 — NC_0_J — 0402

29 TUNER1_SVIN_SNS# — TUNER1_SVIN_SNS# — R623 — NC_0_J — 0402 — SVIN_SNS#
29 TUNER2_SVIN_SNS# — TUNER2_SVIN_SNS# — R624 — NC_0_J — 0402

CN36
HEADER_12P
FOX_HS6112E

1 AUDIO_IN_R
2 AV_IN_GND
3 AUDIO_IN_L
4 AV_IN_GND
5 VIDEO_COMP
6 SVIN_SNS#
7 SVIN_Y
8 AV_IN_GND
9 SVIN_C
10 AV_IN_GND
11 IR_BLASTER 40
12
13
14

AV_IN_GND
AV_IN_GND
AV_IN_GND
AV_IN_GND

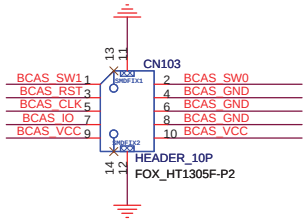
C2343 NC_470P_50V_K_B 0402
C2339 NC_470P_50V_K_B 0402
C2344 NC_470P_50V_K_B 0402
C2340 NC_470P_50V_K_B 0402
C2341 NC_470P_50V_K_B 0402
C2342 NC_470P_50V_K_B 0402

RF SPLITTER POWER

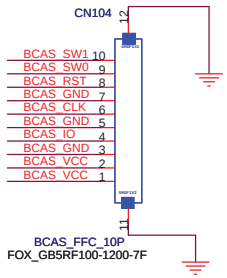
R37966 10K_J 0402
QXH_2
U170
CONTROL
GND
NOISE BYPASS
VIN
VOUT
NJM2877F3-48
QXH_3
5VRUN
C2592 0.1U_16V_Y_Y 0402
+4D8V_SPLITTER
C2594 2.2U_10V_M 0805_X5R
C2593 0402 0.1U_16V_Y_Y
+4D8V_SPLITTER
R37967 10K_F 0402
CN101
HEADER_3P
FOX_HS8103E
RF_SPLITTER_ON_R
R37968 NC_0_J 0402
RF_SPLITTER_ON 21
C2595 2.2U_10V_Y 0603_Y5V
R37969 NC_22K_F 0402
3/29 Change for ME

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AV_IN/SVIDEO IN/RF Splitter Power	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Wednesday, September 17, 2008	Sheet 30 of 77	

B-CAS connentor
(CLOSE TO B_CAS DB)



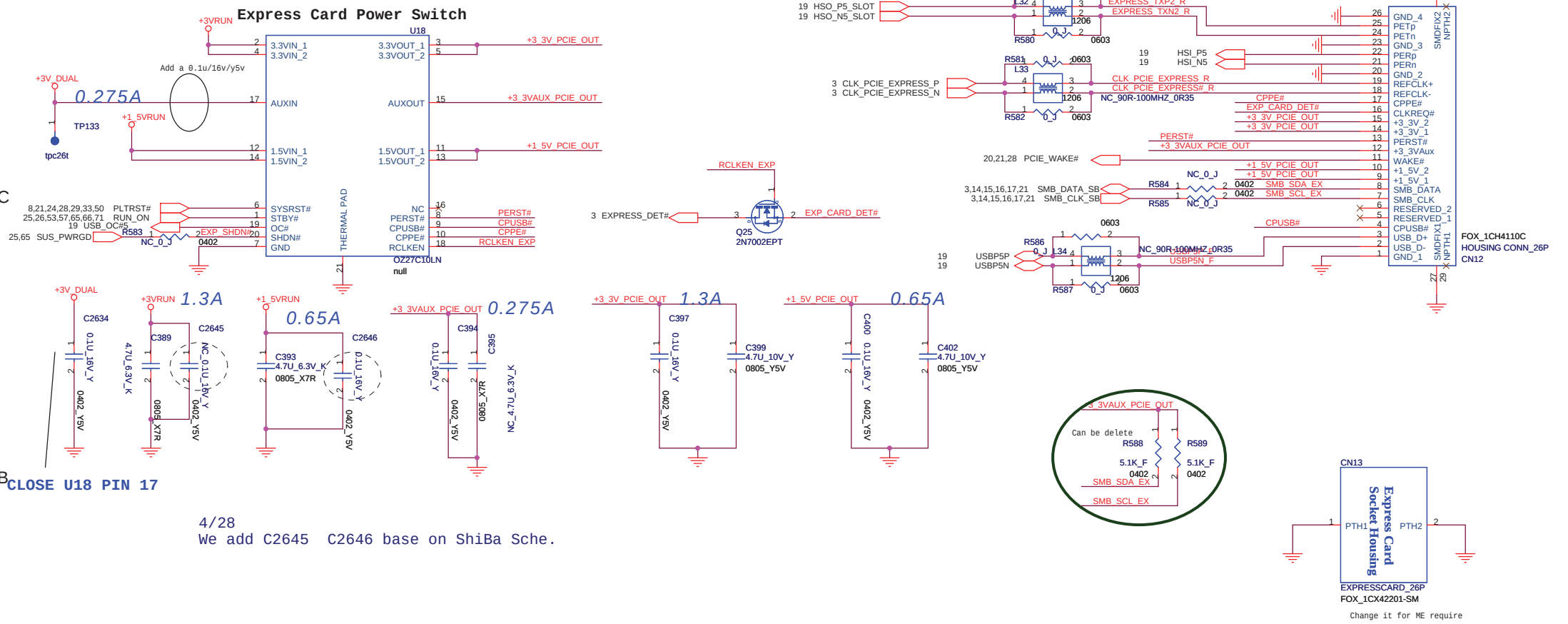
B-CAS connentor
(Close to TV Tuner1 CN68)



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: B_CAS		
Size: A3	Document Number: M841 DVT	Rev: 0.1
Date: Thursday, September 11, 2008	Sheet 31 of 77	

VOLTAGE INPUTS(1)			LOGIC INPUTS			VOLTAGE OUTPUTS(2)			MODE(3)
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP (4)	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

Express Card Power Switch



CLOSE U18 PIN 17

4/28
We add C2645 C2646 base on ShiBa Sche.

Change it for ME require

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	ExpressCard		
Size A3	Document Number M841 DVT		Rev 0.1
Date: Saturday, September 13, 2008	Sheet 32 of 77		

08/01/10: Change from +3VRUN power to +3VRUN_CF power for CF reset timing issue.

08/01/10: Change from +3VRUN power to +3VRUN_CF power for CF reset timing issue.

4/23: CHANGE R626 2 PIN FROM +3VRUN_CF TO +3VRUN_CFCARD

CF Card socket

P21: Change CN24 from 1N-0050000-FWN0 to 1N-0050002-MWN0

4/23: CHANGE U25 14 PIN FROM NC TO CF_RST#

9/11: Add F26(NC) for CF test debug

08/01/14: Add those two RESET IC to control the delay time: JMB368 reset 370ms after CF CARD inset, CF CARD reset 792ms after JMB368 reset.

08/01/10: Delete R637 C496 for CF timing issue

4/23: ADD +3VRUN_CFCARD POWER TO CF CARD SLOT

4/23: CHANGE U165 2 PIN FROM +3VRUN_CF TO +3VRUN_CFCARD

3/31,08: Delete pullup res R37929 and R37930 by JMICRON' suggestion.

CompactFlash power circuit

Here we make a option if JMB368 is NOT powered ON without CF media.

4/23: CHANGE R3833 FROM NC TO MOUNT
CHANGE R? FROM MOUNT TO NC

4/23: ADD THIS CIRCUIT FOR CF CARD RESET

Close to IC JMB368

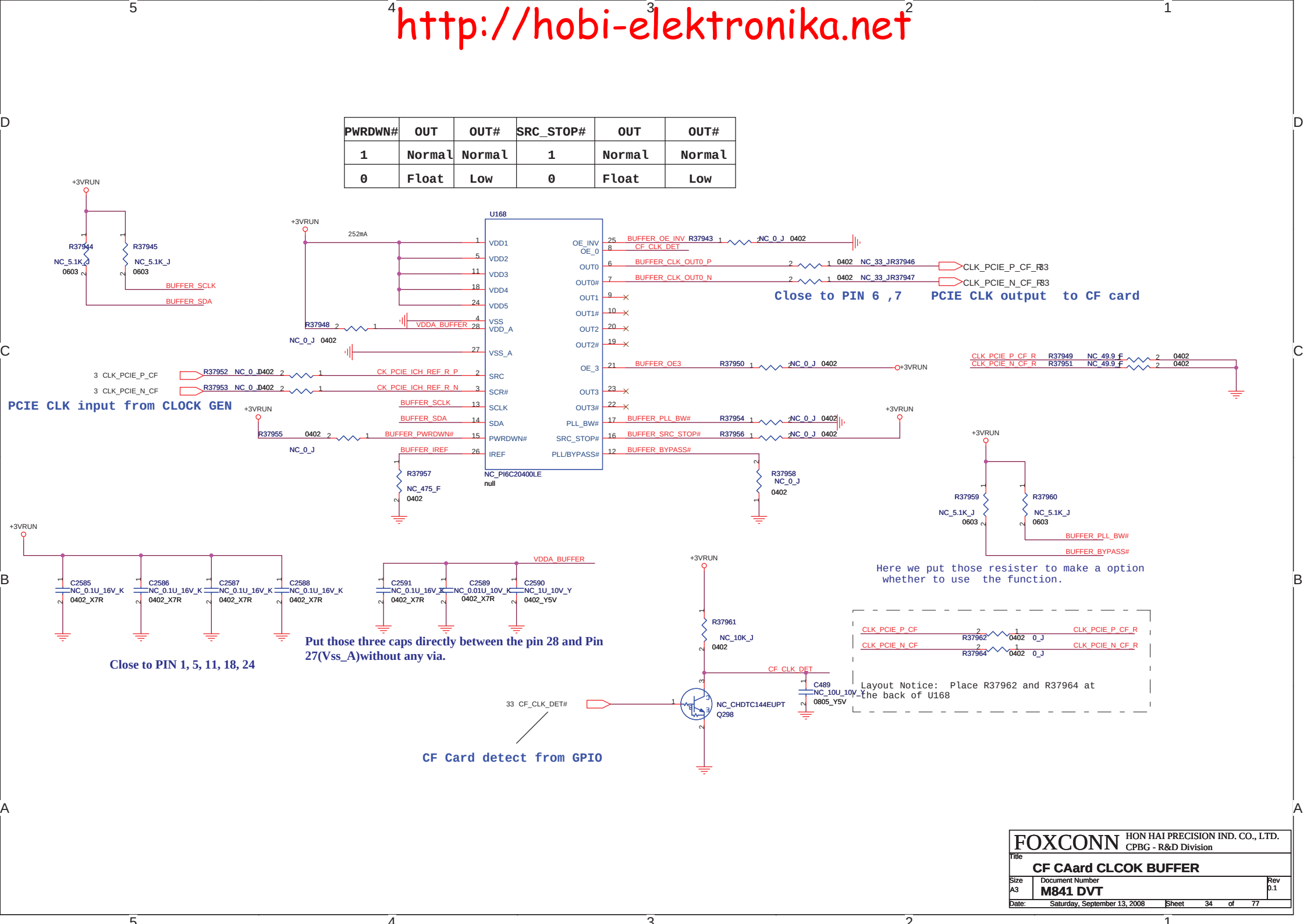
Close to IC JMB368

CLOSE PIN 9

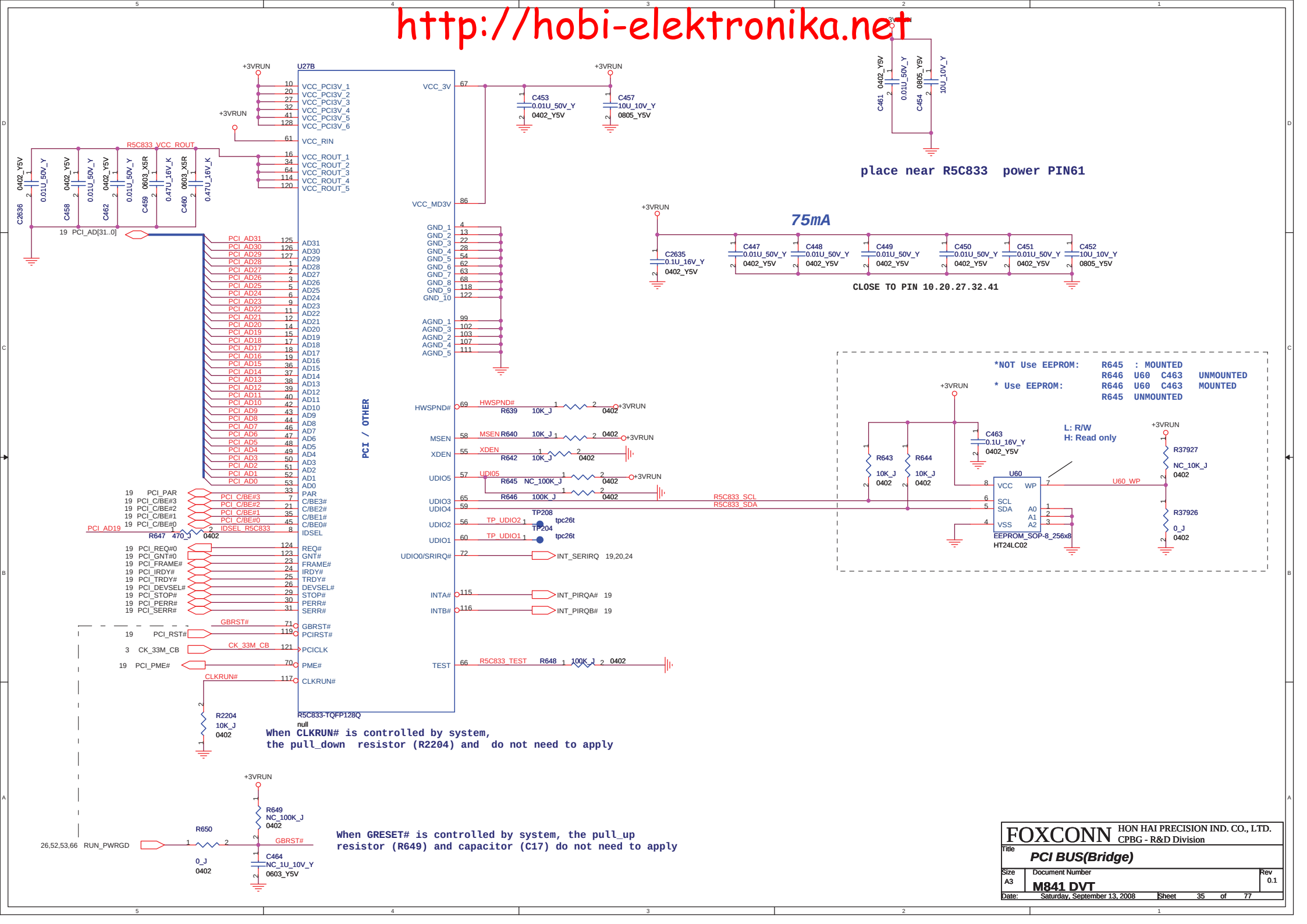
CLOSE PIN 4

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCIE(CF Card)	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Wednesday, September 17, 2008	Sheet 33 of 77	

PWRDWN#	OUT	OUT#	SRC_STOP#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	Float	Low	0	Float	Low



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CF CAard CLCOK BUFFER
Size A3	Document Number M841 DVT
Rev	0.1
Date:	Saturday, September 13, 2008
Sheet	34 of 77



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI BUS(Bridge)	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 35 of 77	

MS/SD POWER

as close as possible to R5c

as close as possible to 1394 connector

Place U61 near MS/SD CONN

250mA

iLink CONN.

SD/MMC CONN.

MS STD/DUO CONN.

AS CLOSE AS POSSIBLE TO R5C833

C476 place near R5c833

C471 place near R5c833

circuit area:as small as possible

Analog GND

IEEE1394/SD

PIN NAME	TYPE	Description
VERF	I/O	VOLTAGE REFERENCE: It is necessary to connect a capacitor of 0.01uF between this pin and AGND.
REXT	I/O	RESISTANCE EXTERNAL: It is necessary to connect a resistor of 10k ±1% between this pin and AGND.
XI	IN	X'TAL IN: 24.576MHz
XO	OUT	X'TAL OUT: 24.576MHz
FIL0	I/O	FILTER: This pin is used for the PLL Filter. Keep this pin openbecause it is notnecessary for the R5C833 to use this pin.

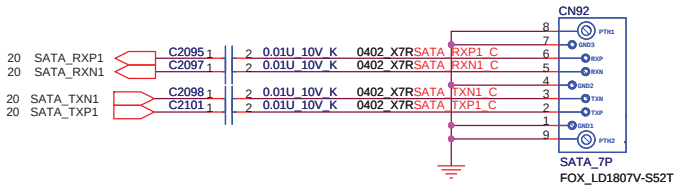
Place near SD socket

Place near MS socket

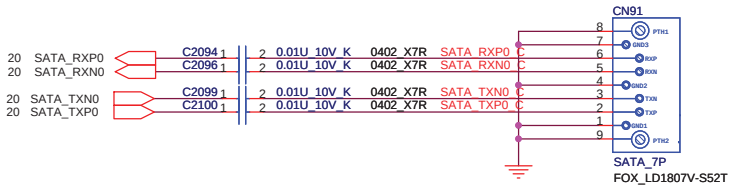
1/3 08
Add capacitor to follow EMI suggest

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCIBUS(MS&SD&iLink)
Size A3	Document Number M841 DVT
Rev	0.1
Date:	Saturday, September 13, 2008
Sheet	36 of 77

HDD2

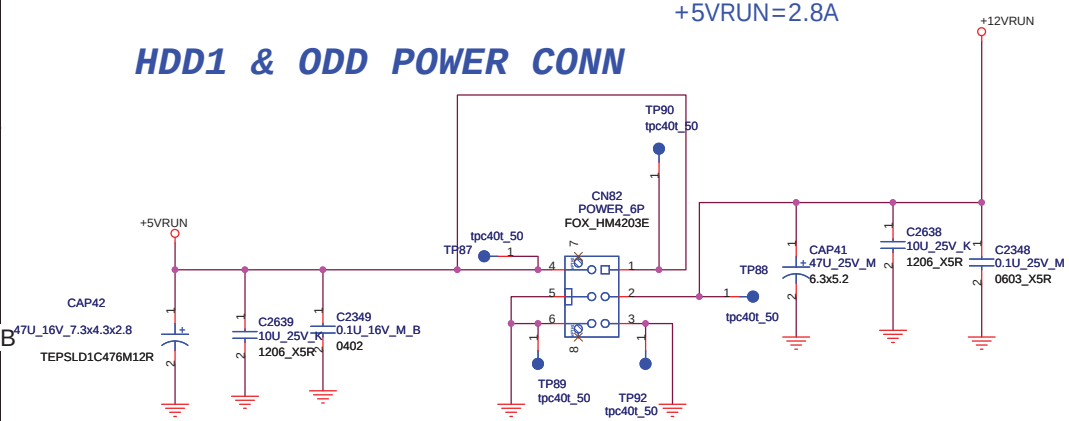


HDD1



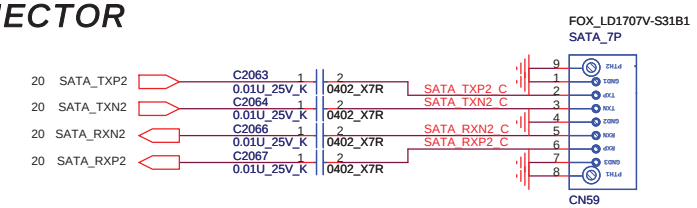
Power Budget
+12VRUN=4A, PEAK,4SECONDS
+5VRUN=2.8A

HDD1 & ODD POWER CONN



4/28 :change pin 2 from +12VRUN to GND,chane pin 5 from GND to +5VRUN

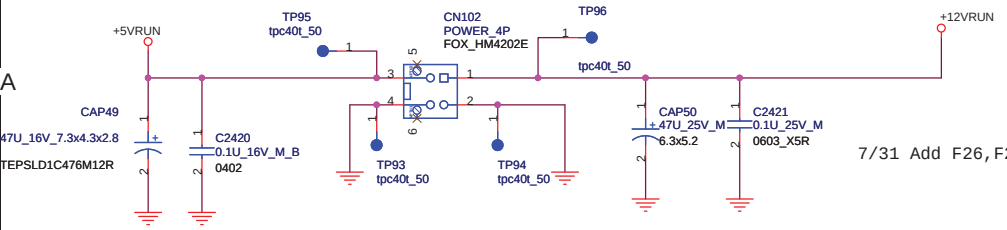
SATA ODD CONNECTOR



SATA ODD and SATA HDD share the same POWER CONN.

Power Budget
+12VRUN=4A, PEAK,4SECONDS
+5VRUN=0.8A

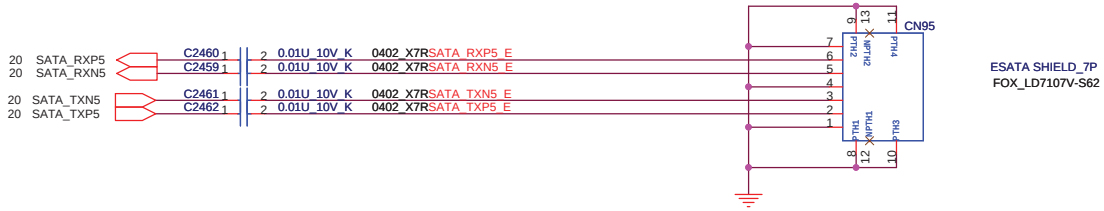
HDD2 POWER CONN



7/31 Add F26,F27

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SATA HDD&ODD	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 37 of 77	

eSATA



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: eSATA		
Size: A3	Document Number: M841 DVT	Rev: 0.1
Date: Saturday, September 13, 2008	Sheet 38 of 77	

NOTE:S0,S1,S3

+5V_DUAL

500mA
F2
6V_2.6A_1812
miniSMDC260F-2

VCC_G545_IN

C2014
1U_25V_M_B
0603

U118
GND OUT_3
IN_1 OUT_2
IN_2 OUT_1
EN(EN#) OC#
G545B1P8U

C2012 0402
0.1U_16V_Y_Y

USB_VCC0

USB_OC#0 19

41,44,45,53,65,71,72 SUS_ON

USB Port on Board

R678
0_J 0603 1206
L40
NC_90R-100MHZ_0R35
0_J 0603
R680

19 USBP0P
19 USBP0N

USBP0P_F
USBP0N_F

USB_VCC0
R679 0_J 0805
USB_VCC0_R
USBP0N_F
USBP0P_F

CAP8
+150U_6.3V_M
3528

C2013
470P_50V_K_B
0402_X7R

D11
NC1
NC2
NC_RSB12JS2

CN70
USB_4P
FOX_UB11193-C1304-4F

USB DB CONN

4/16:Add F24

F24
6V-0.35A_1206
1206L035
+3V_DUAL

F6
6V_2.6A_1812
miniSMDC260F-2
+5V_DUAL

C2519
1U_10V_Y
0603_Y5V

4/28:delete c2547,add c81

C2523
0.1U_16V_Y
0402

C81
10U_10V_Y
0805_Y5V

1/3
Add to follow EMI suggest

CN57
HEADER CONN_20P
FOX_HT1310F

19 USB_OC#3
19 USB_OC#4
19 USBP4N
19 USBP4P
SUS_ON
19 USBP3N
19 USBP3P

VCC_USB_F6

BIND_RF# 41
BT_WLAN_ON# 44
WLAN_BT_SW# 20,28,40
WLAN_BT_OFF 21

R38016
SYS_LED
150_J
0402

Q217
2N7002EPT

4/16:Del R38016,R2355,R2354,U129 FOR SYSTEM LED

EN_POWER_1
EN_POWER_1 53,56,57,58,71

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	USB Port &CONN	
Size A3	Document Number M841 DVT	Rev 0.1
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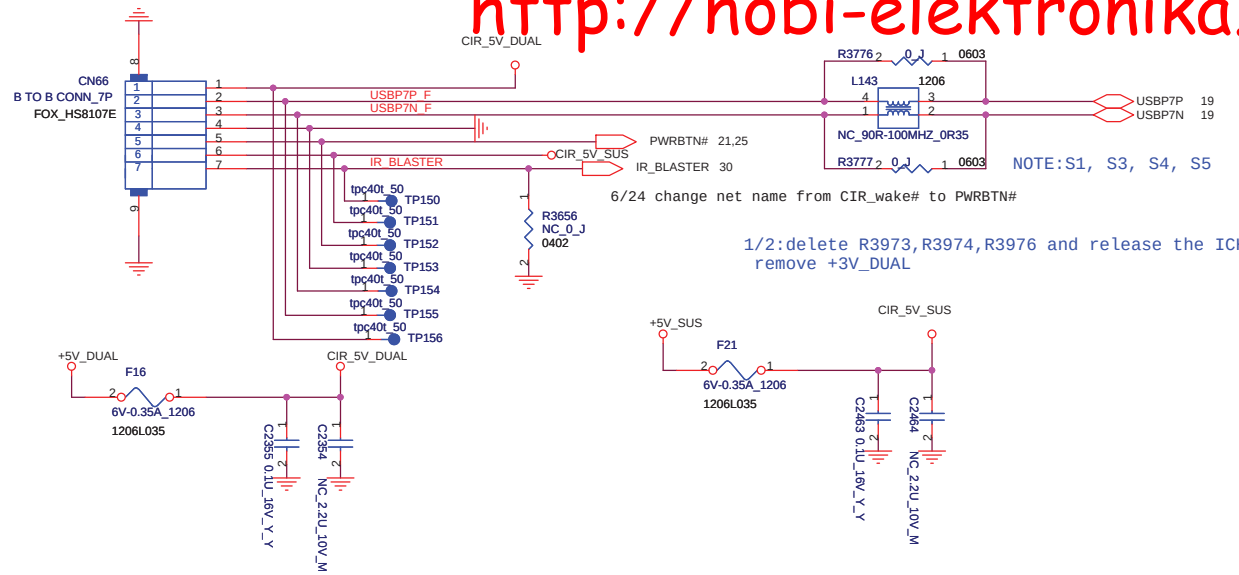
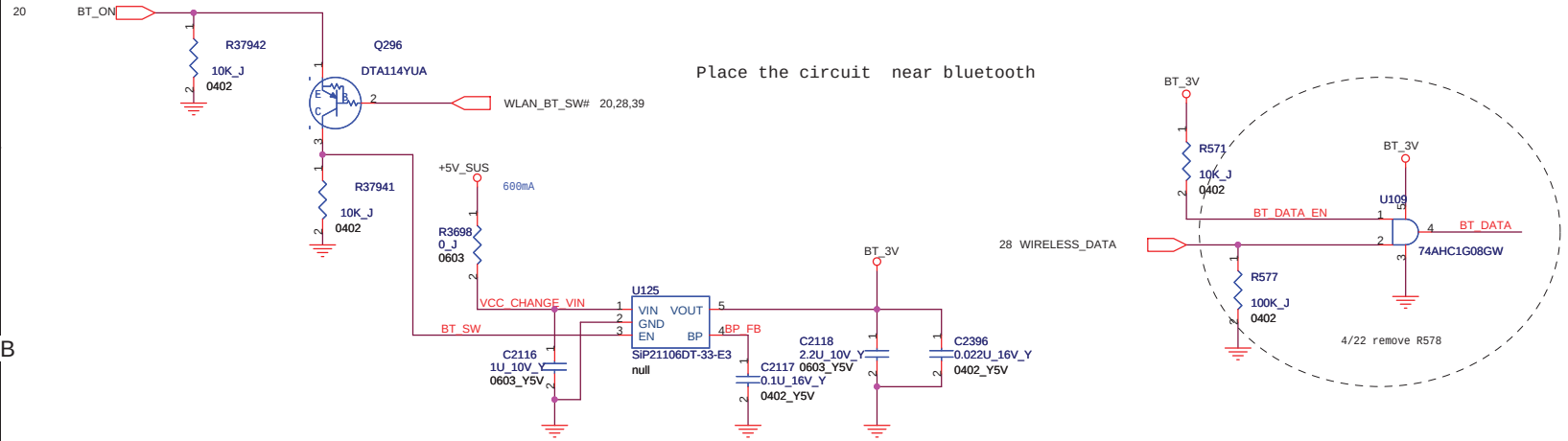
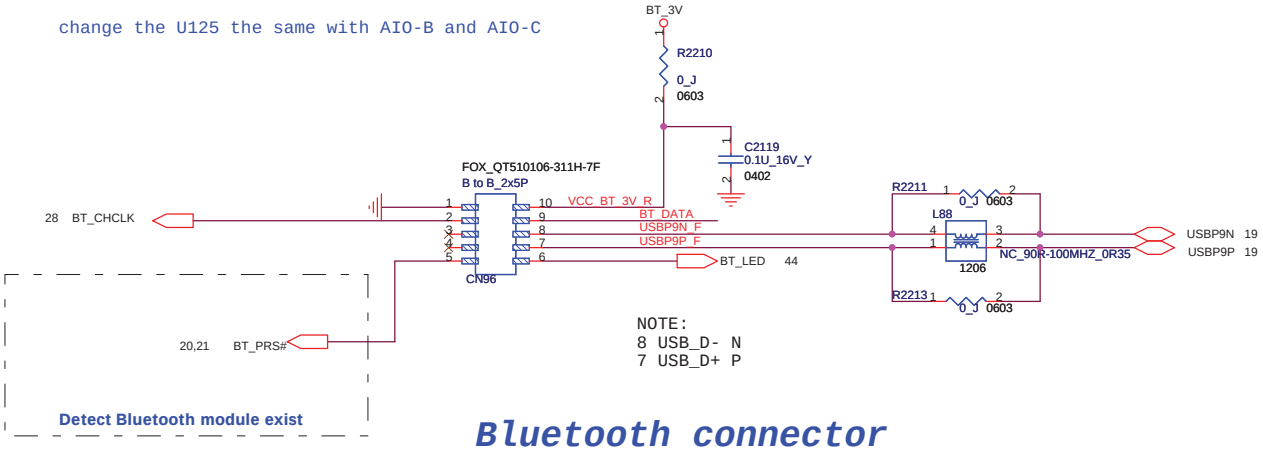
CIR





change the U125 the same with AIO-B and AIO-C



Bluetooth connector

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CIR&BT
Size	A3
Document Number	M841 DVT
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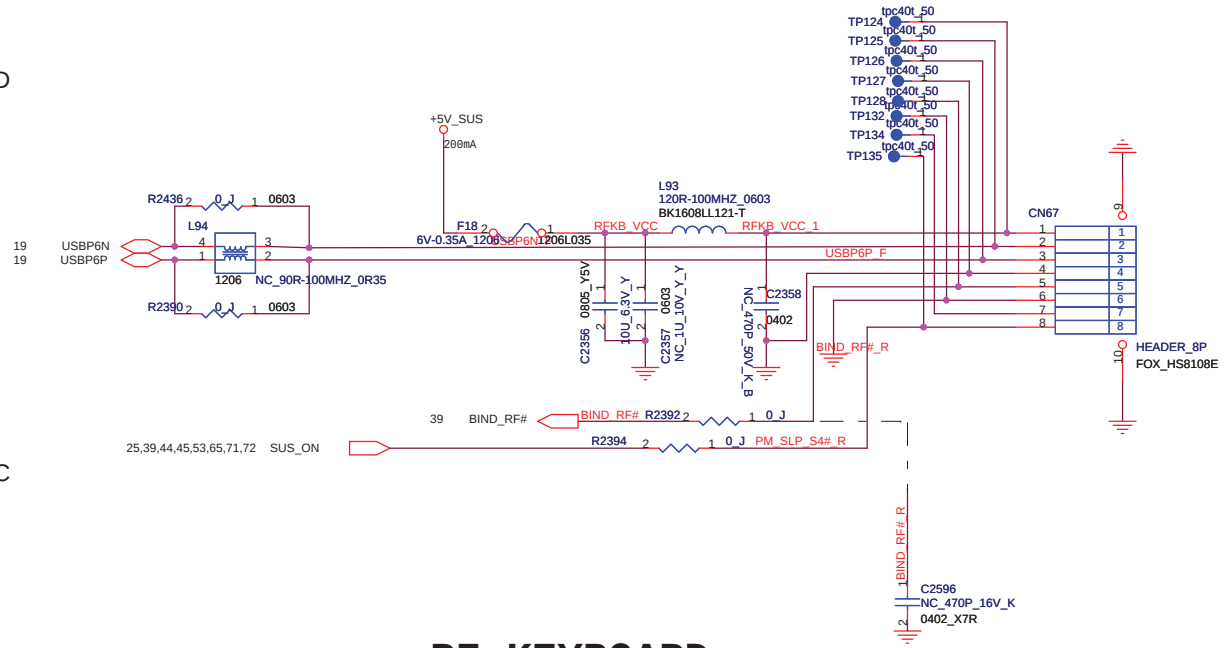
1/2:change to +5V_DUAL for supporting the S4/S5 wake from RF KBD



NOTE:S1, S3, S4, S5

PWR_RF#:reserved for RF wake up from S4/S5

RF KEYBOARD

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: RF KB CONN		
Size: A3	Document Number: M841 DVT	Rev: 0.1
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INVERTER

SPS

ADD
ADDR_SEL SMBUS ADDRESS
'0' (GND) 0101_111xb

The THRM# signal is used as a status input for a thermal sensor. Based on the THRM# signal going active, the ICH10 generates an SMI# or SCI (depending on SCI_EN).

DDR & TVTUNERTEMP SENSOR Address
ADD0 ADD1
0 0 0x48
MXM THERMAL SENSOR ADDRESS
ADD1 ADD0 ADDRESS
FLOAT HIGH OX4D

caps C2182, C2184 and C2186, 2200pF is 470pF would be a good value and be placed close to the EMC2106 pins

NOTE:PWM4
configurations for PWM4 as backlight control
- set Reg0E0h B[6:5]="11b" to select pin5 as PWM4
- config Reg2Bh B[7:6] to select PWM4 base freq
- config Reg2Fh for PWM4 Divide for exact freq
- set Reg2Eh for PWM4 duty cycle
SHDN_SEL (pin22) and SYS_SHDN# (pin 9), you may leave them as NC

2007/12/31
delete R2355/R2336/R2357/R3341 10K resistor

DESIGN NOTE:
DDR & TVTUNERTEMP SENSOR

CAD NOTE:
PLACE CAP NEAR SST SENSOR PINS

NOTE: PLACE NEAR TVTUNER

CAD NOTE:
PLACE SST SENSOR NEAR DDR ,opposite to the cpu plane

4/14 NC R37916, it has been pulled high on page 5

4/16 NC Q165 R168,

3/21:add R2353 for pull up

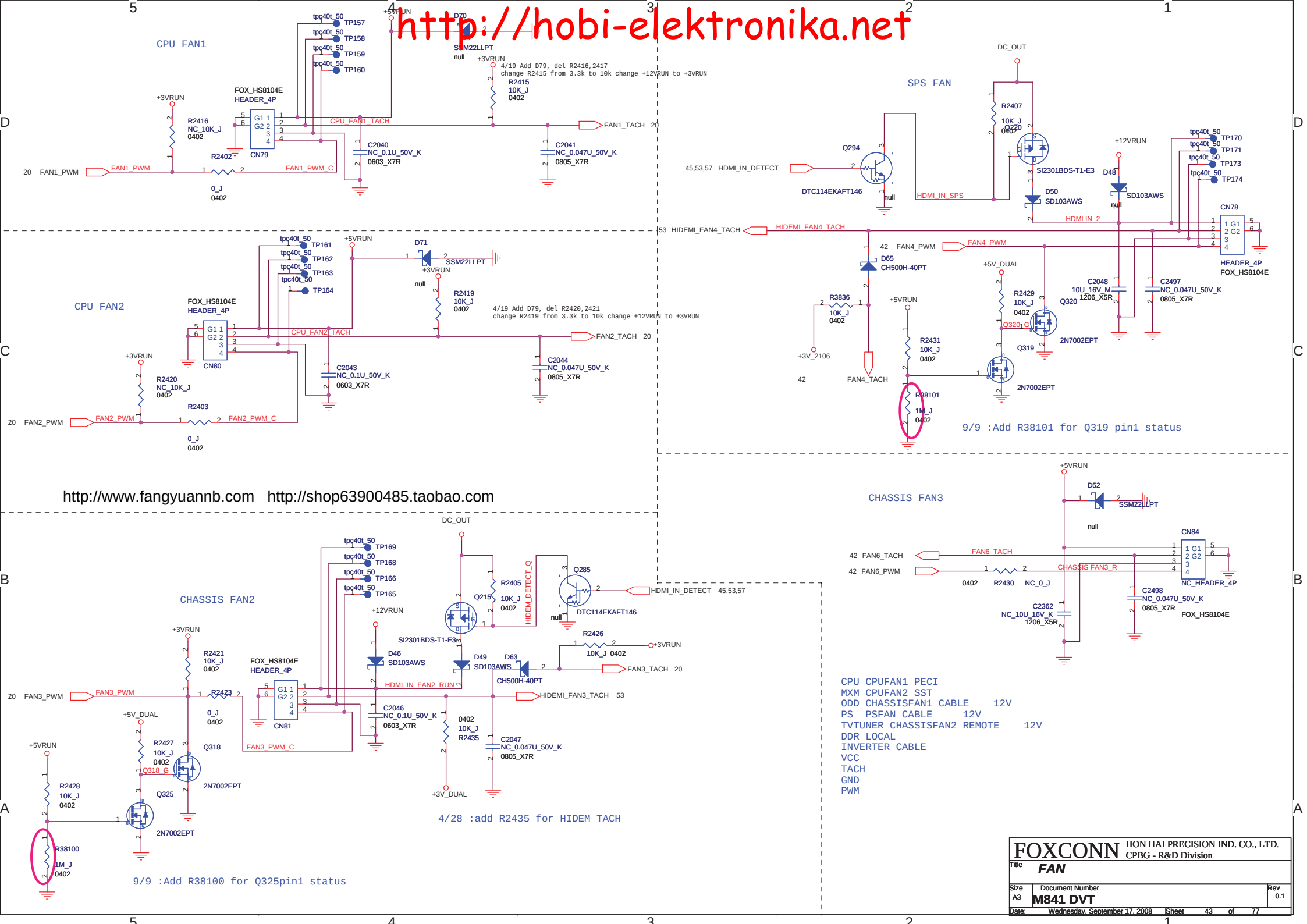
HW THERMAL PROTECTION

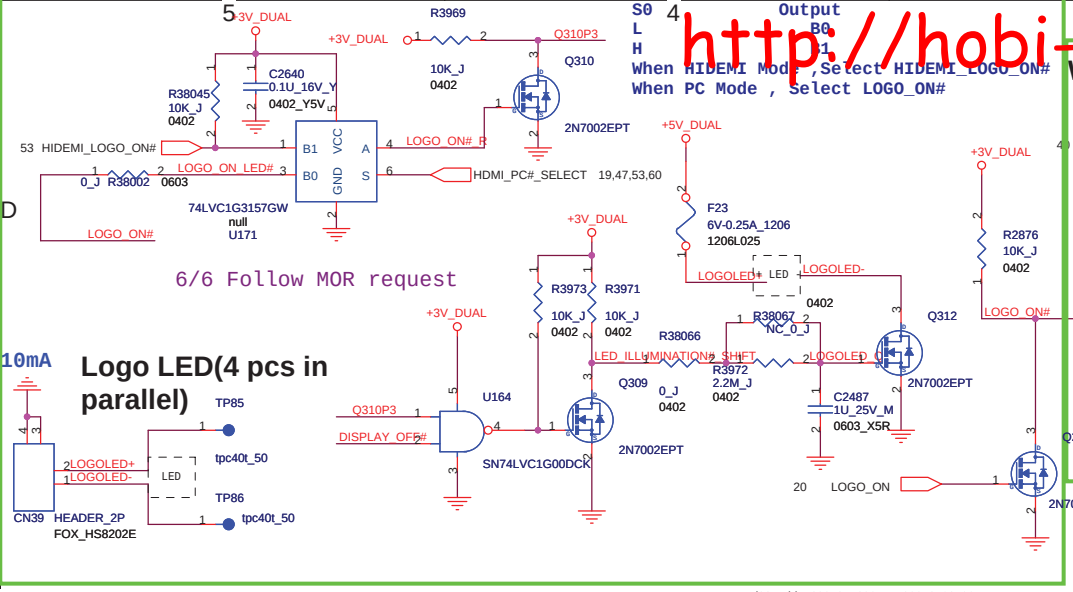
HW thermal shut down temperature setting 95 degree . Put Near CPU .

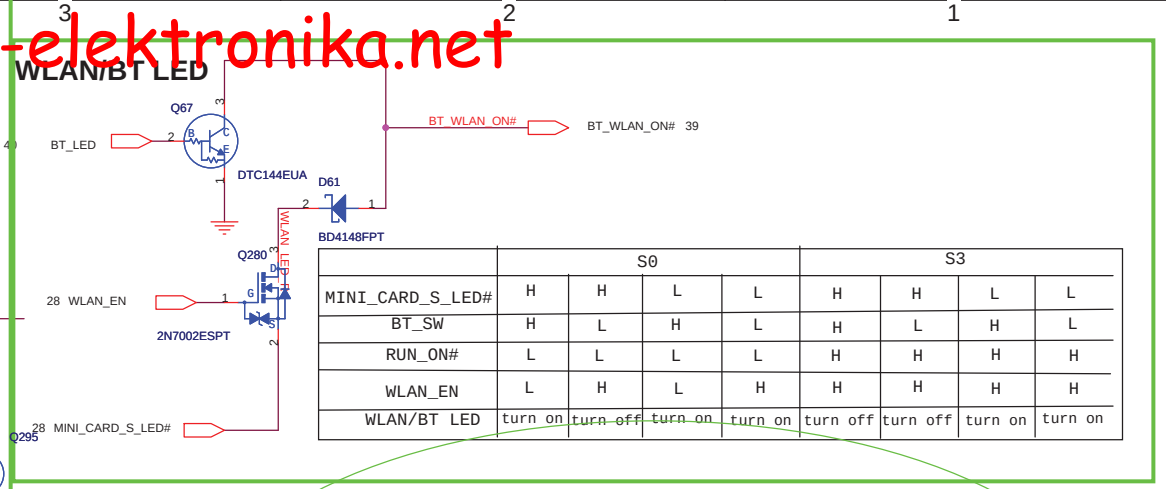
PIN1 SET:Temperature Set Point. Connect an external 1% resistor from SET to GND to set trip point.
To set the temperature trip point from 0°C to +125°C, use the following equation:
RSET = [(8.3793 · 104) / T] - 211.3569 +[(1.2989 · 105) / T2]=289k
where T is the trip temperature in Kelvin.

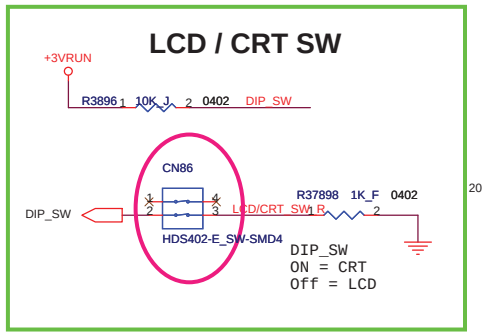
The EMC2101 is addressed on the SMBus as 100_1100b.

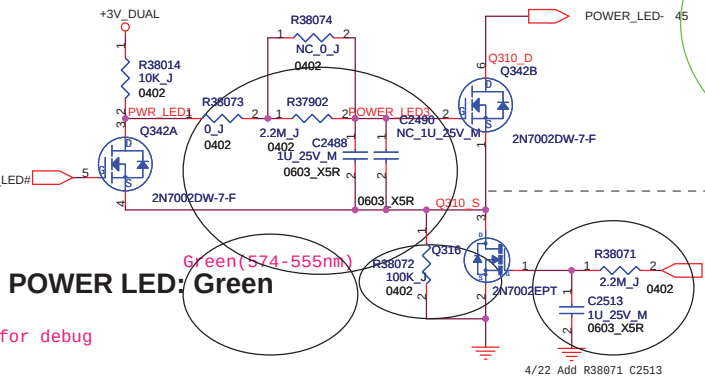
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Thermal & BL
Size A3	Document Number M841 DVT
Rev	0.1
Date: Saturday, September 13, 2008	Sheet 42 of 77

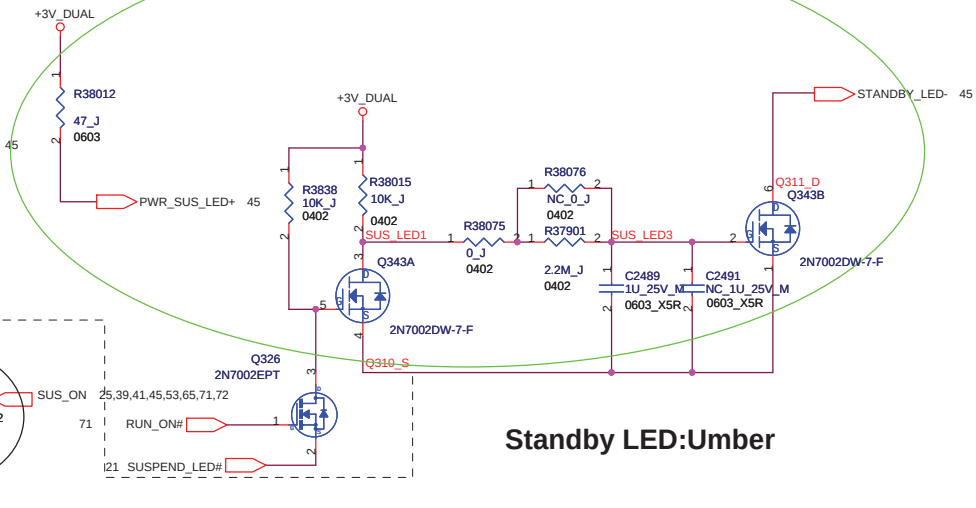


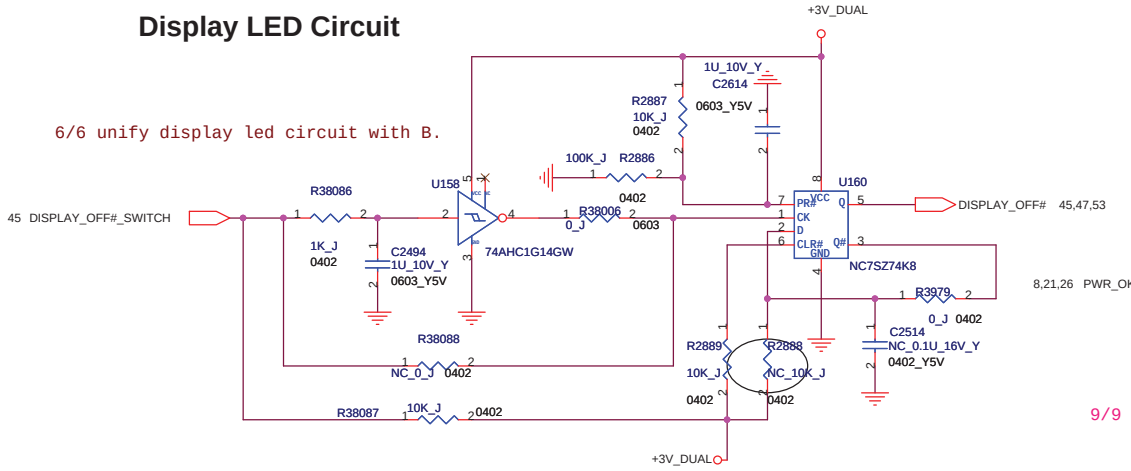


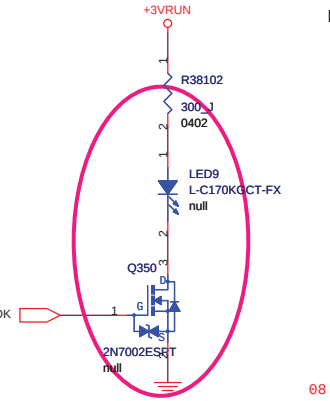


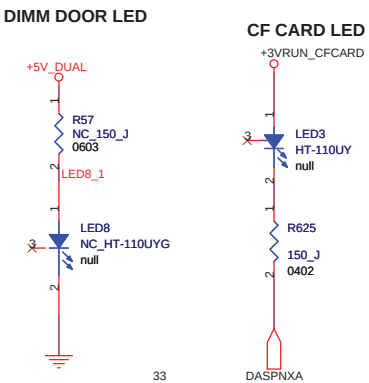


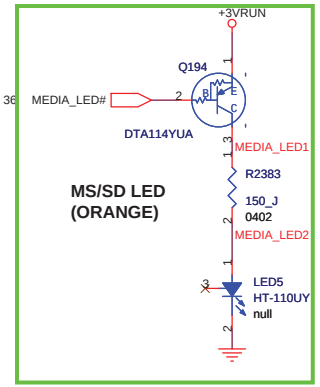












9/9 Add R38102,LED9,Q350 for debug

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: LED

Size: A3 | Document Number: M841 DVT | Rev: 0.1

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RJ45/SPDIF/USB CONN

12/24 07 : Analog 2CH and Side 10 pin incorporate to one DB "IO DB"

1000mA FOR TWO USB CONN

CN98

HEADER CONN_30P
FOX_HT1315F

30mA FOR SPDIF

+5V_DUAL

1000mA FOR TWO USB CONN

D51 SSM22LLPT null

C2376 0.1U_16V_M_B 0402

C2377 0.1U_16V_M_B 0402

CAP47 +NC_47U_16V_M 5x5.2

C2378 10U_10V_M 0805_X5R

I/O DB CONN

http://www.fangyuannb.com http://shop63900485.taobao.com

Power Supply CONN

4/16 Change GND to SPS_GND

4/16 change PS_ON# to AC_OFF# for PUS pin define change

CN90 HEADER_2x9P FOX_HM4209E

CHASSIS FAN1

1/3
Add to follow EMI suggest

Power Switch CONN

DC_OUT

Q216 CHT84PT

R2406 10K_J 0402

Q288 CHDTC144EUPT

HDMI_IN_DETECT 43,53,57

HDMI_DET_FAN5_DC

CN100_P13

CN100

D47 SD1030WS

D64 CH500H-40PT

R3834 10K_J 0402

R37931 10K_J 0402

R3835 NC_10K_J 0402

C2049 10U_16V_K 1206_X5R

C2496 NC_0.047U_50V_K 0805_X7R

HEADER CONN_20P FOX_HT1310F

C2564 1U_10V_K 0603_X5R

C15 0.1U_16V_Y 0402_Y5V

4/21 add C15 for EMI

R38042 NC_680_J 0402

Q344 DTA114YUA

R38043 150_J 0402

Q322 SI2304BDS-T1-E3

Q321 SI2304BDS-T1-E3

R2432 10K_J 0402

R2433 10K_J 0402

Q327 DTA114YUA

R38044 56_J 0402

03/11 Add these circuits because move power switch board circuit to MB

8/2 change R38044 from 1R-0000151-J200 to1R-0000560-J200

6/12 Add CN106 for ME change

CN106 HEADER_2P FOX_HS8102E

R2434 NC_10K_J 0402

R38058 NC_0_J 0402

R38057 NC_0_J 0402

Q328 NC_IRLML5103TRPbF

C2550 0.1U_50V_K 0603_X7R

C2551 0.1U_50V_K 0603_X7R

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	DB CONN(PSwitch/PSP/IO)
Size A3	Document Number M841 DVT
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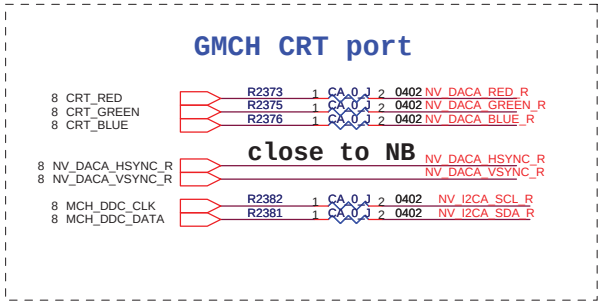

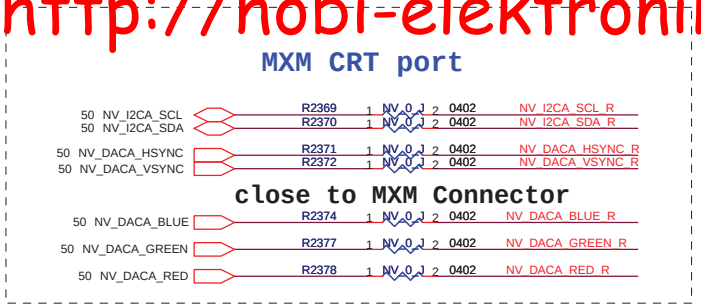

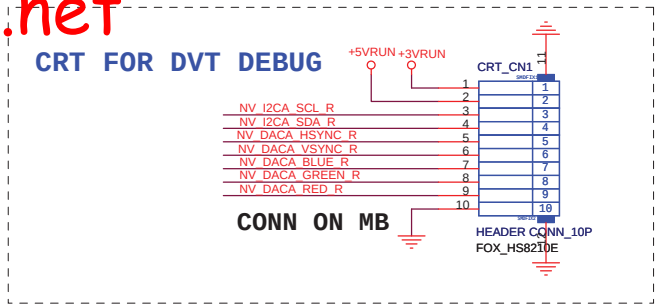

Change history of VGA portion from page 46 to page 53 (base on M840 MP)

DVT

0821

1,Stuff CRT

2,Change NV_thermal_alert connect from AC_OFF_3# to ICH H_THERMTRIP#

0909

1.Change CN53 pin assignment for HIDEMI,
change pin 14 from GND to SUS_ON;
change Pin 18 from GND to INV_BRADJ;
change Pin 40 from TP to INV_ENABLE1;
change Pin 39 from GND to HIDEMI_DETECT;
Add R38108 1M ohm for HIDEMI_DETECT PD.

2,change page 46 LVDS SW selector from HDMI_PC#_SELECT to HIDEMI_DETECT

0911

1,Page 53 add Back up circuit for HIDEMI2 compatibility with HIDEMI 1 FW.

2,CN53 change Pin 32 from gnd to LCDVCC_EN;

0912

1,Add a AND gate for HIDEMI_SUS_ON;

2,Change the signal net name from HIDEMI_DETECT to HIDEMI_EXIST and HIDEMI_DETECT_CN to HIDEMI_EXIST_CN;

3,Add back up RUN_ON signal to HIDEMI;

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CRT (FOR DEBUG)		
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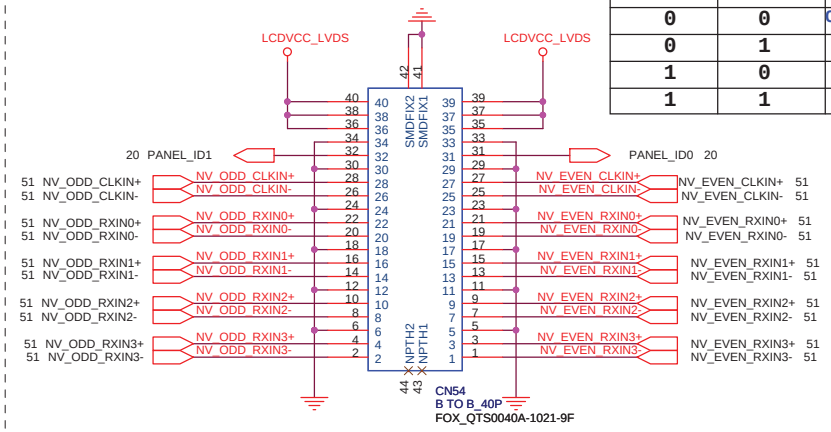
LVDS

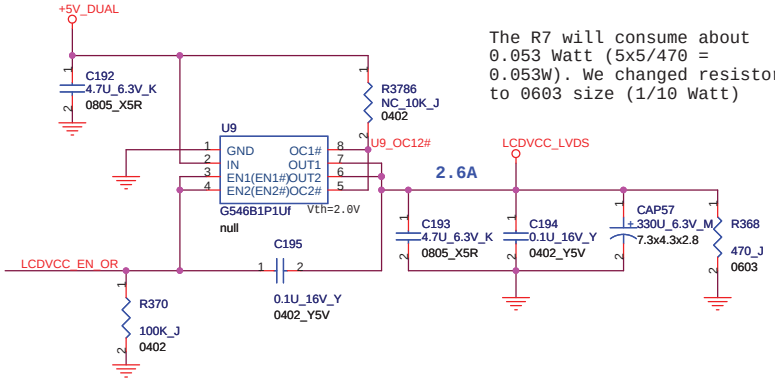
M840 26" Panel ID Table

PANEL_ID1	PANEL_ID0	Type 1	Type 2	Type 3	Type 4
0	0	CLAA260WU11			
0	1		Reserve		
1	0			Reserve	
1	1				Reserve

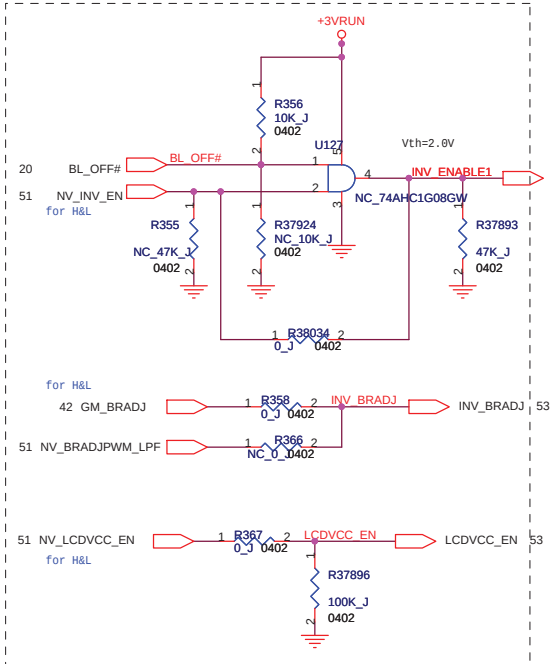


LVDS CONNECTOR

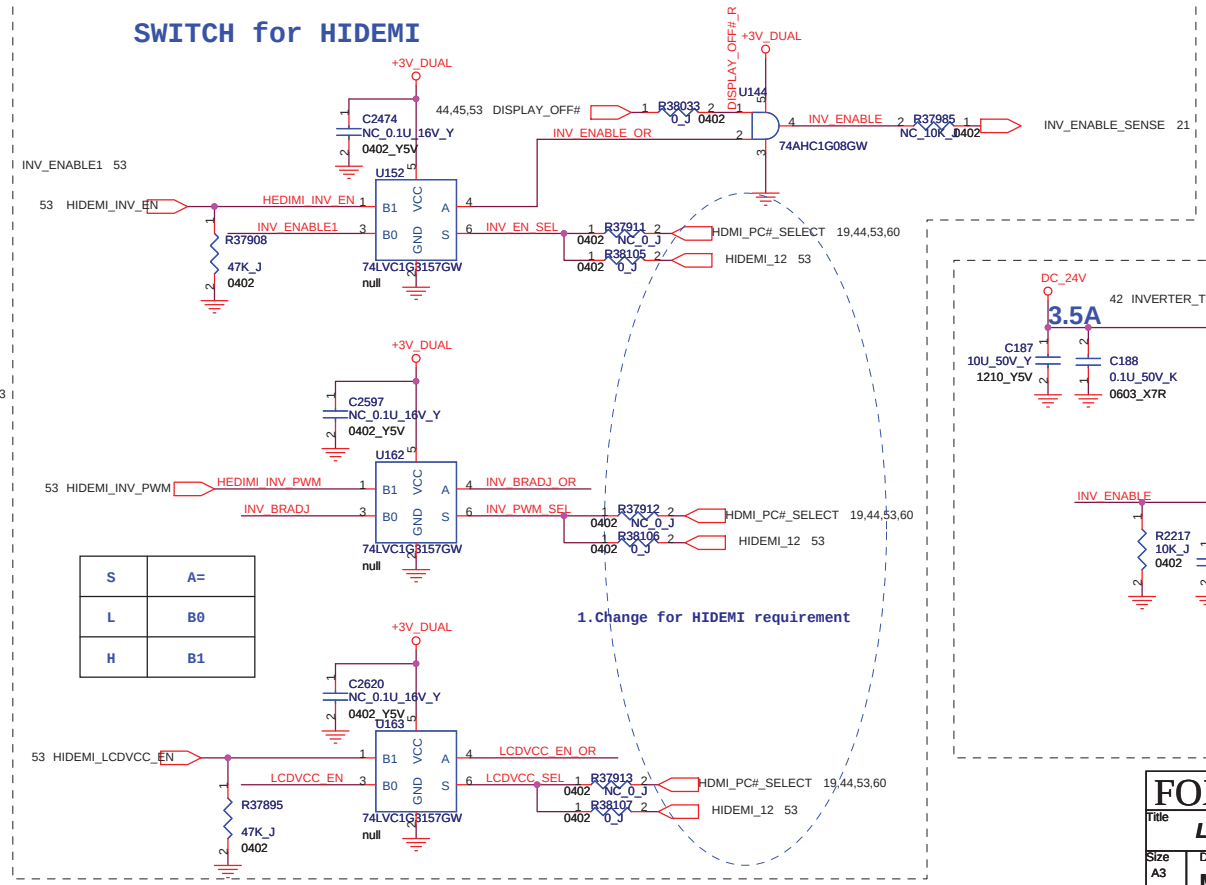
LCD POWER LATCH

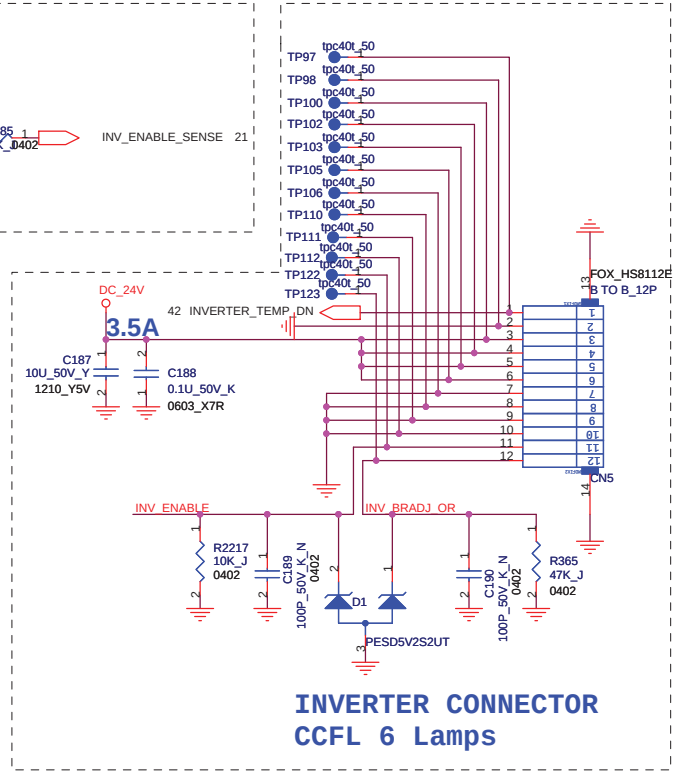


The R7 will consume about 0.053 Watt (5x5/470 = 0.053W). We changed resistor to 0603 size (1/10 Watt)



SWITCH for HIDEMI





INVERTER CONNECTOR
CCFL 6 Lamps

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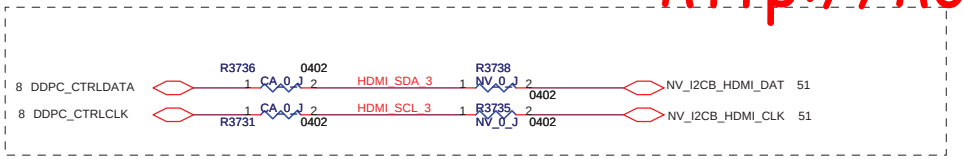

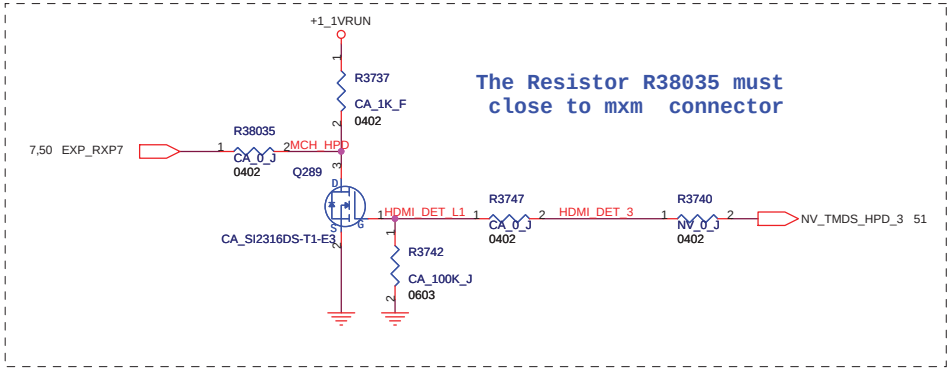

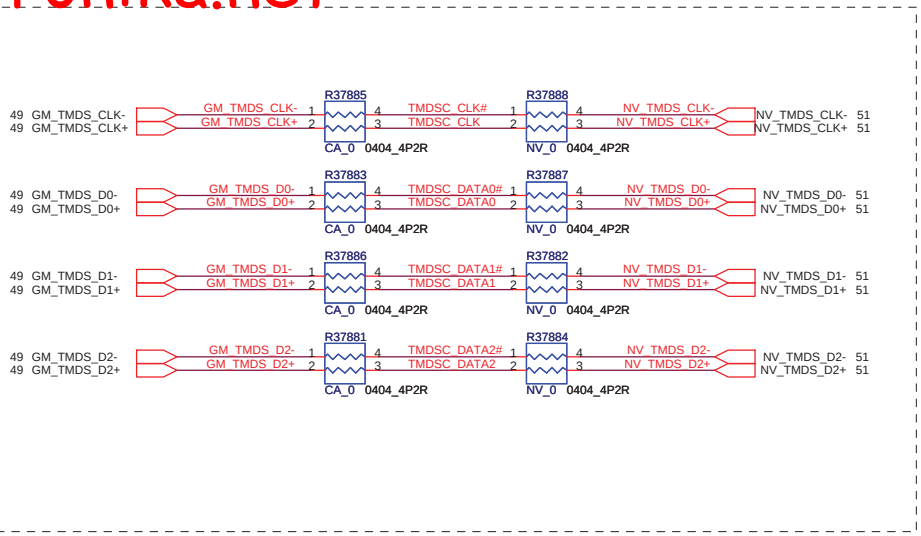

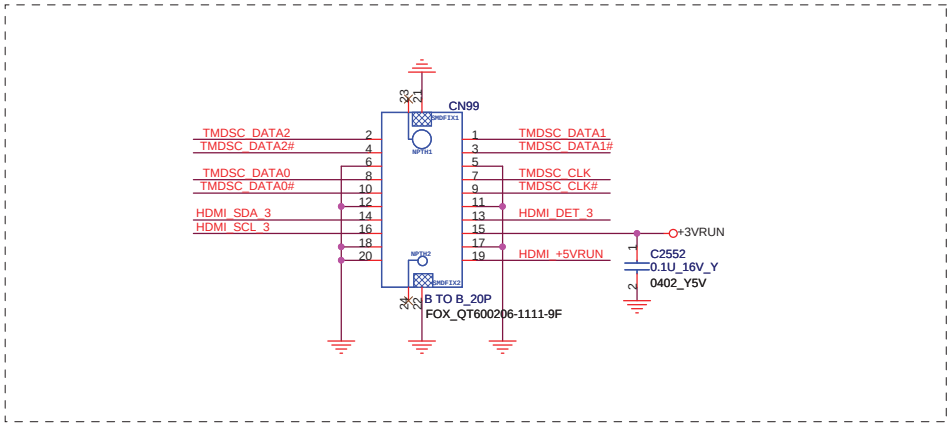

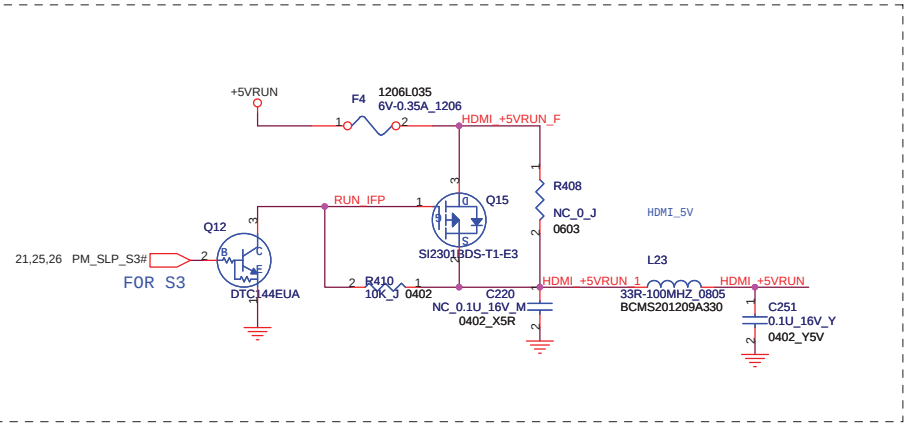

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **HDMI OUT**

Size: A3 | Document Number: **M841 DVT** | Rev: 0.1

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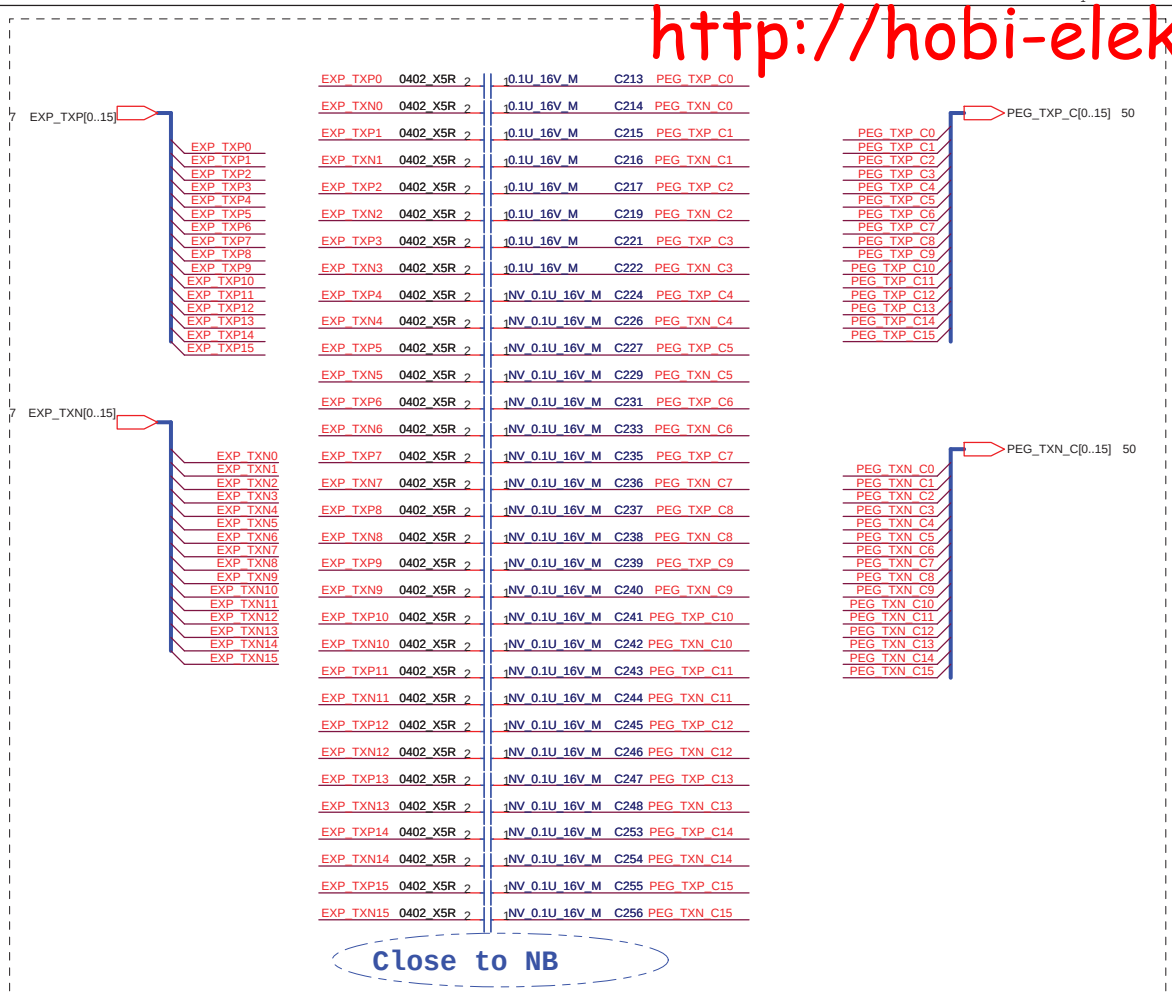

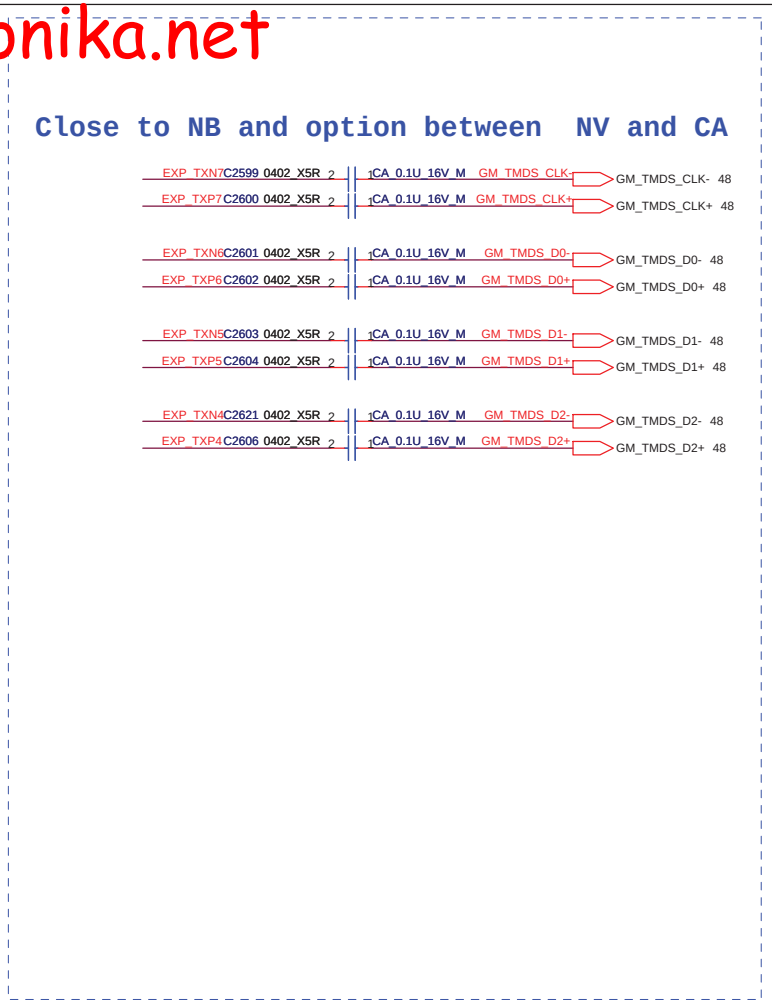

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCIE SWITCH	
Size A3	Document Number M841 DVT	Rev 0.1
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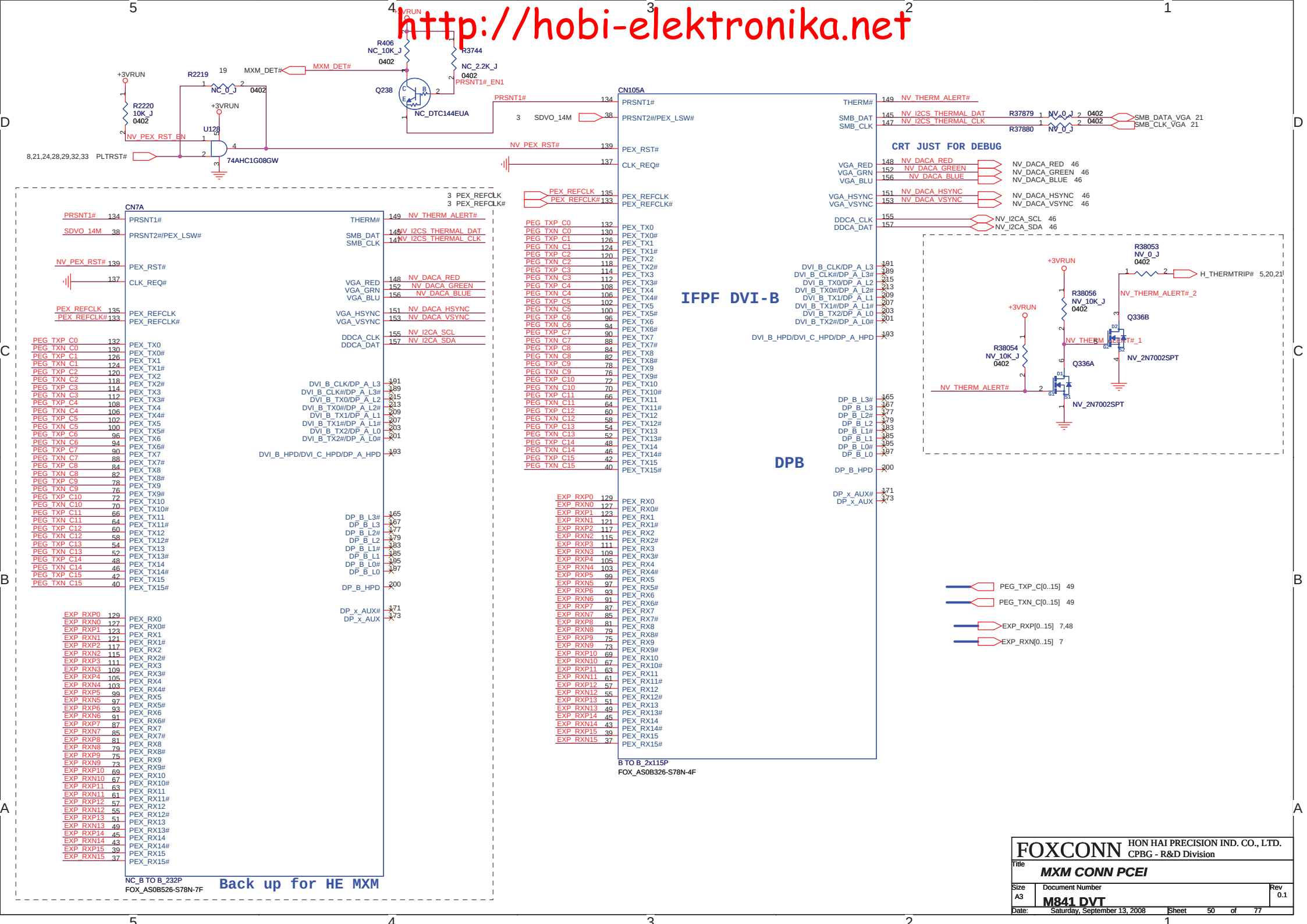

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	MXM CONN PCEI
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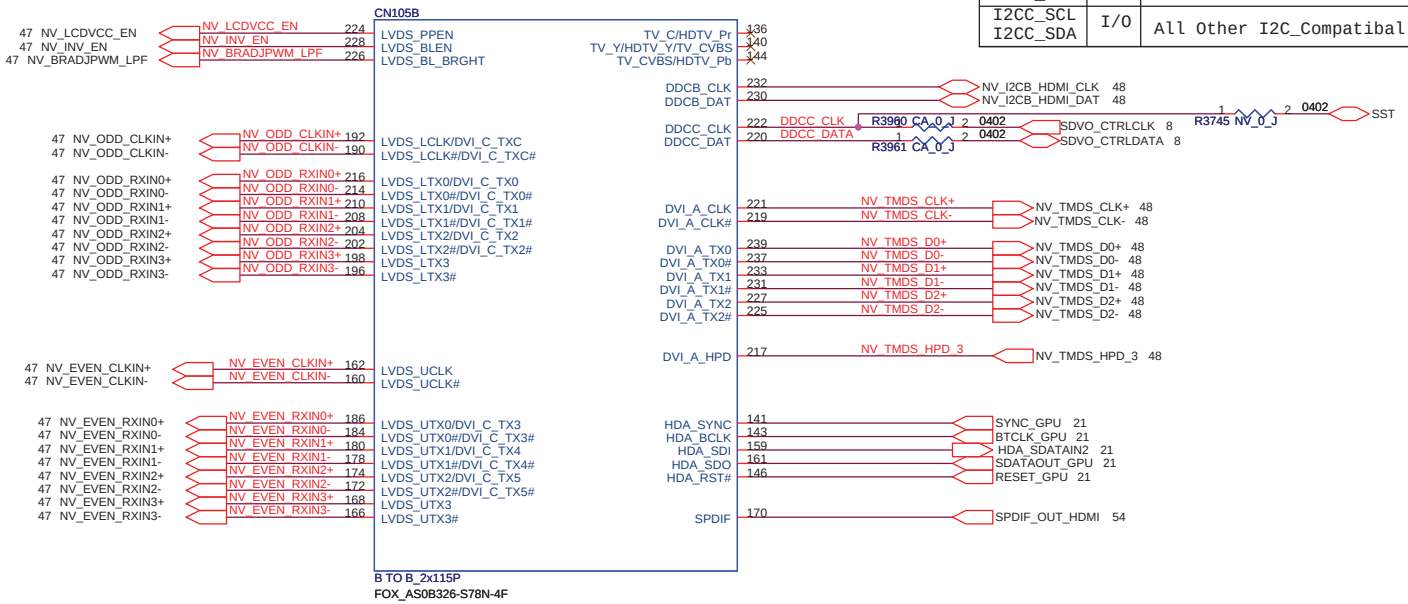
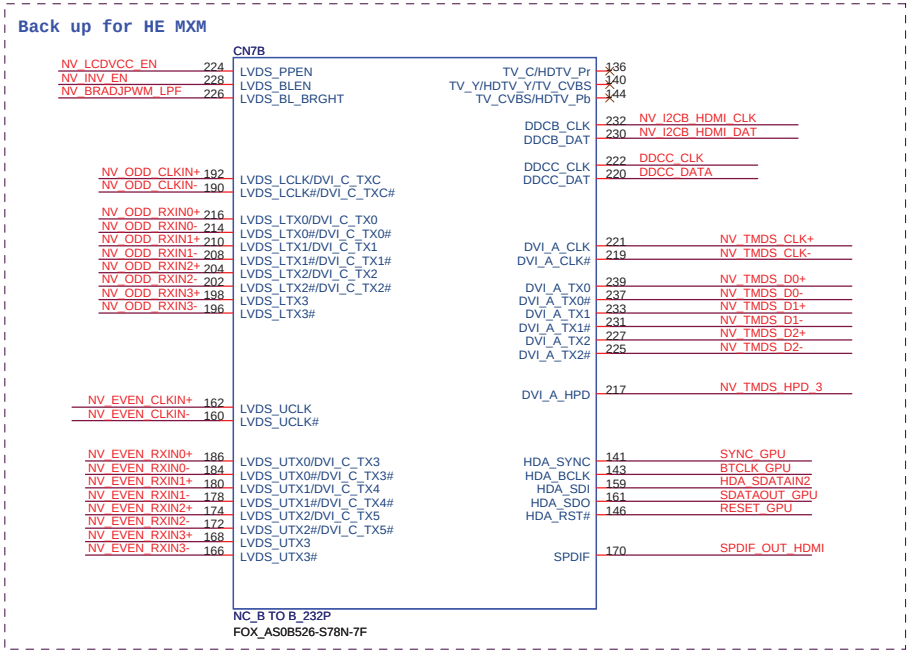
SIGNAL	I/O	Description	Used for
I2CA_SCL I2CA_SDA	I/O	Notebook VGA I2C_Compatibal Bus Signals	DAC A DDC BUS
I2CB_SCL I2CB_SDA	I/O	Notebook HDMI I2C_Compatibal Bus Signals	HDMI DDC BUS
I2CC_SCL I2CC_SDA	I/O	All Other I2C_Compatibal Bus Signals	SDVO CONTROL BUS/SST

MXM_SST
ADD0:HIGH
ADD1:FLOATING
ADDRESS:0x4D

SDVO DDC_AS STRAP=HIGH
High Device Address is 70h.
low Device Address is 72h.



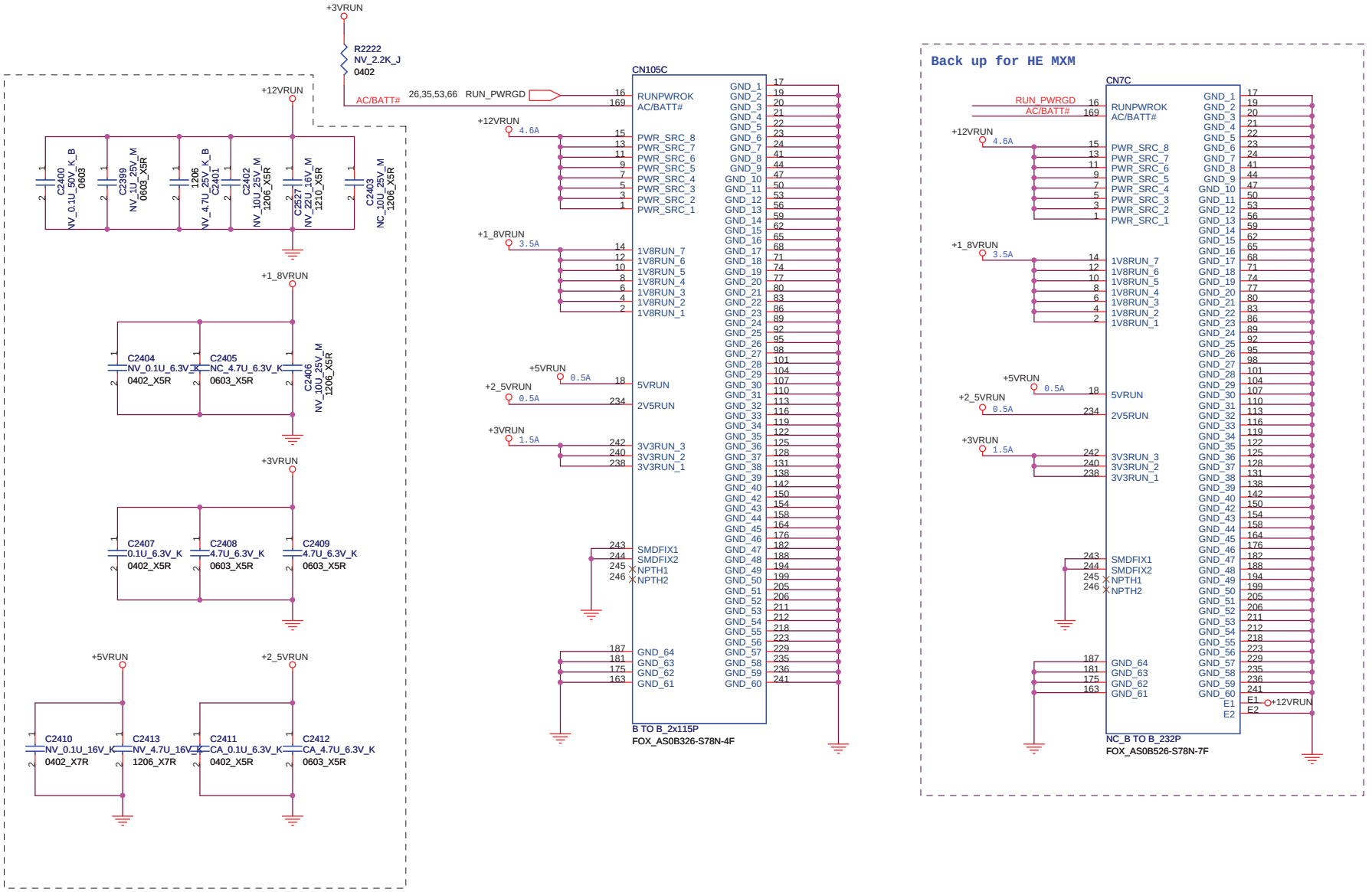


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **MXM CONN OUT**

Size: A3 | Document Number: **M841 DVT** | Rev: 0.1

Date: Saturday, September 13, 2008 | Sheet 51 of 77



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **MXM CONN POWER**

Size	Document Number	Rev
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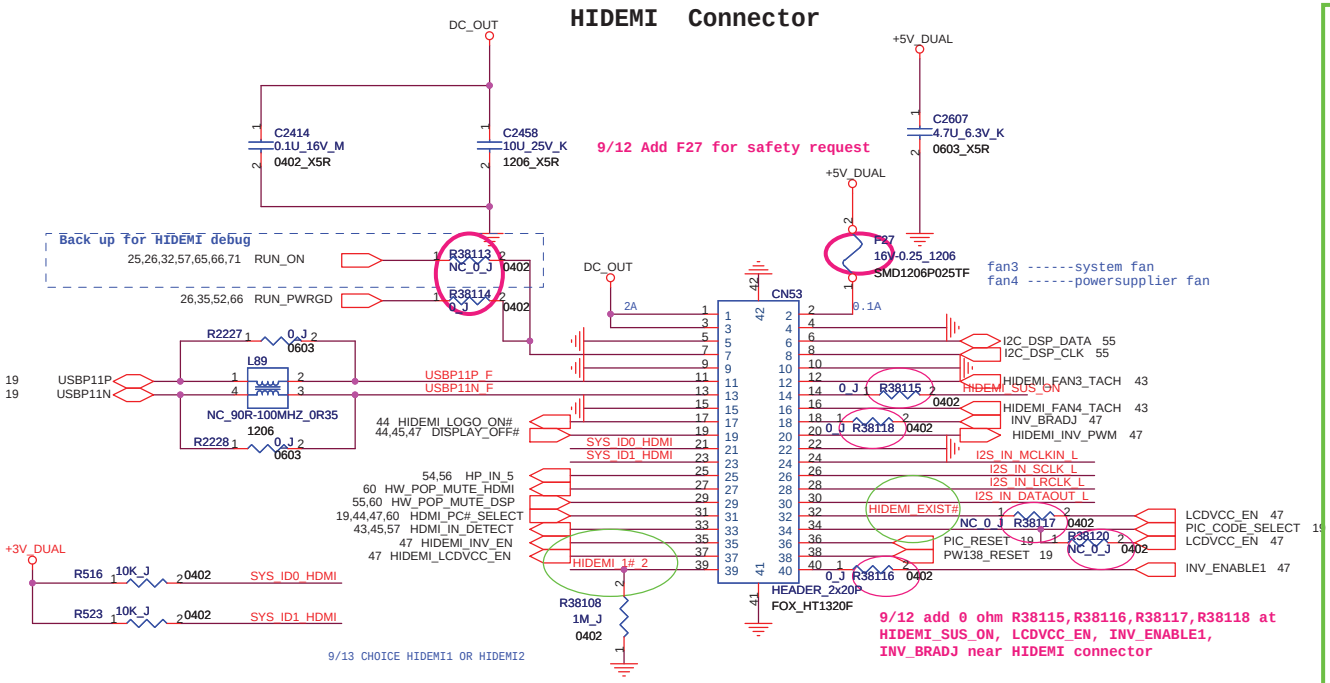
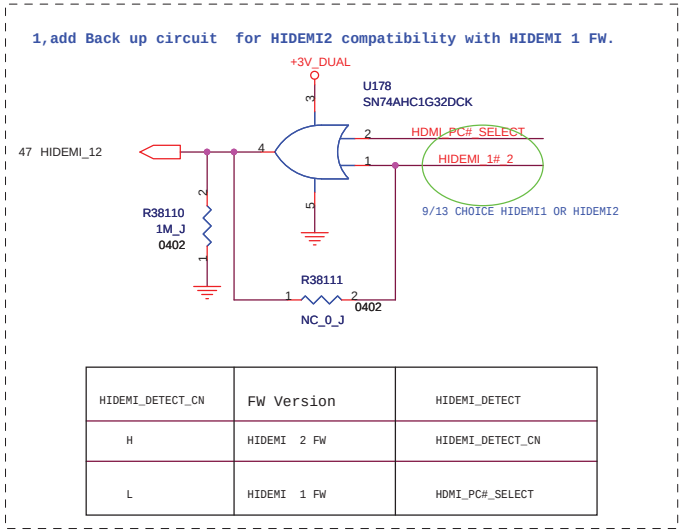
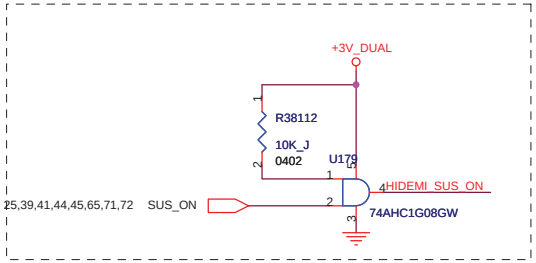
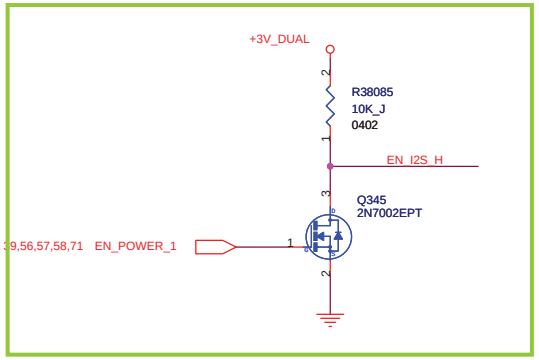
HIDEMI Connector

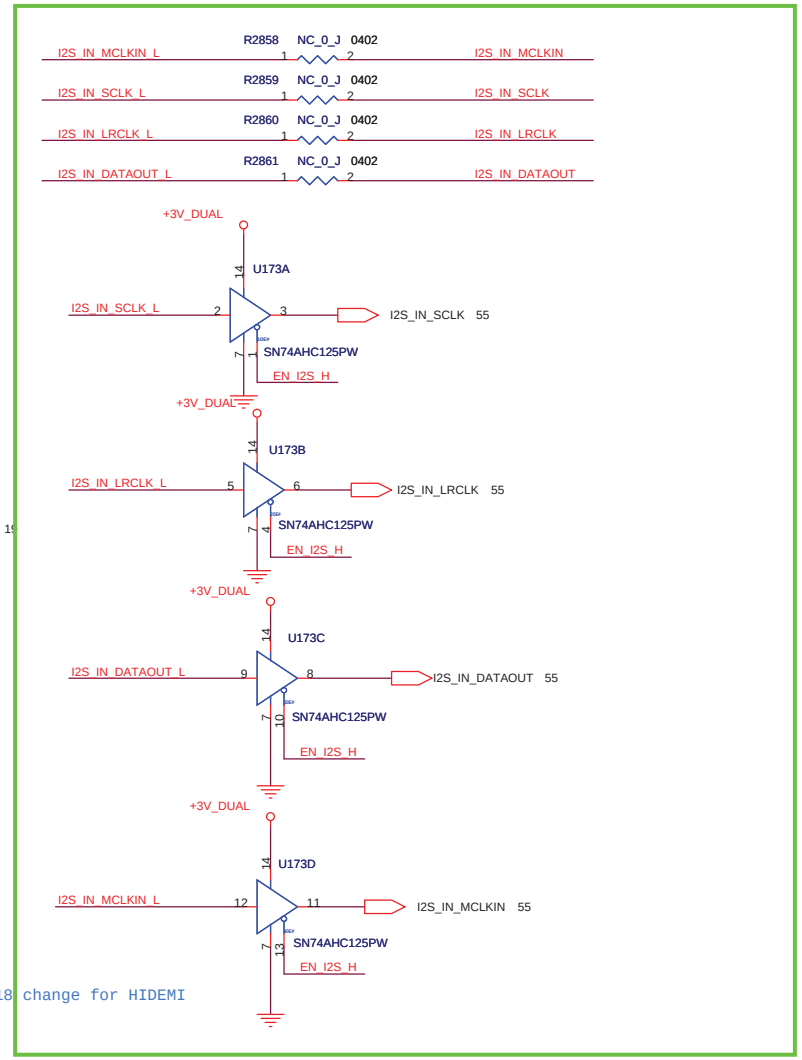




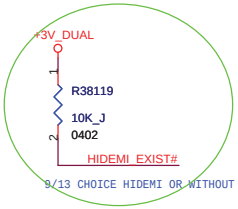
HIDEMI_DETECT_CN	FW Version	HIDEMI_DETECT
H	HIDEMI 2 FW	HIDEMI_DETECT_CN
L	HIDEMI 1 FW	HDMI_PC#_SELECT







4/18 change for HIDEMI



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA MB TO HIDEMI CONN

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0131
C1856 change from 1U_6.3V to 10U_6.3V
place this 2 capacitors near AVDD2(38)

Place near Codec

Place near Codec

Place C1863 Close CODEC.

0911 NC U155,change R827 from 33K_J to 22k_J,
add R38109 (0ohm) for cost down

PC BEEP

R831 ,R832 and R833 Place near SENSE _A Pin

ALC262D Use

ALC889S Use

ALC262D Use

ALC889S Use

TO I/O CONN

Remove SPDIF OUT CONN to DB.

4.75V/0.2A

0131
Place this 2 capacitors near AVDD1(25)

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Title	AUDIO(CODEC & POWER)
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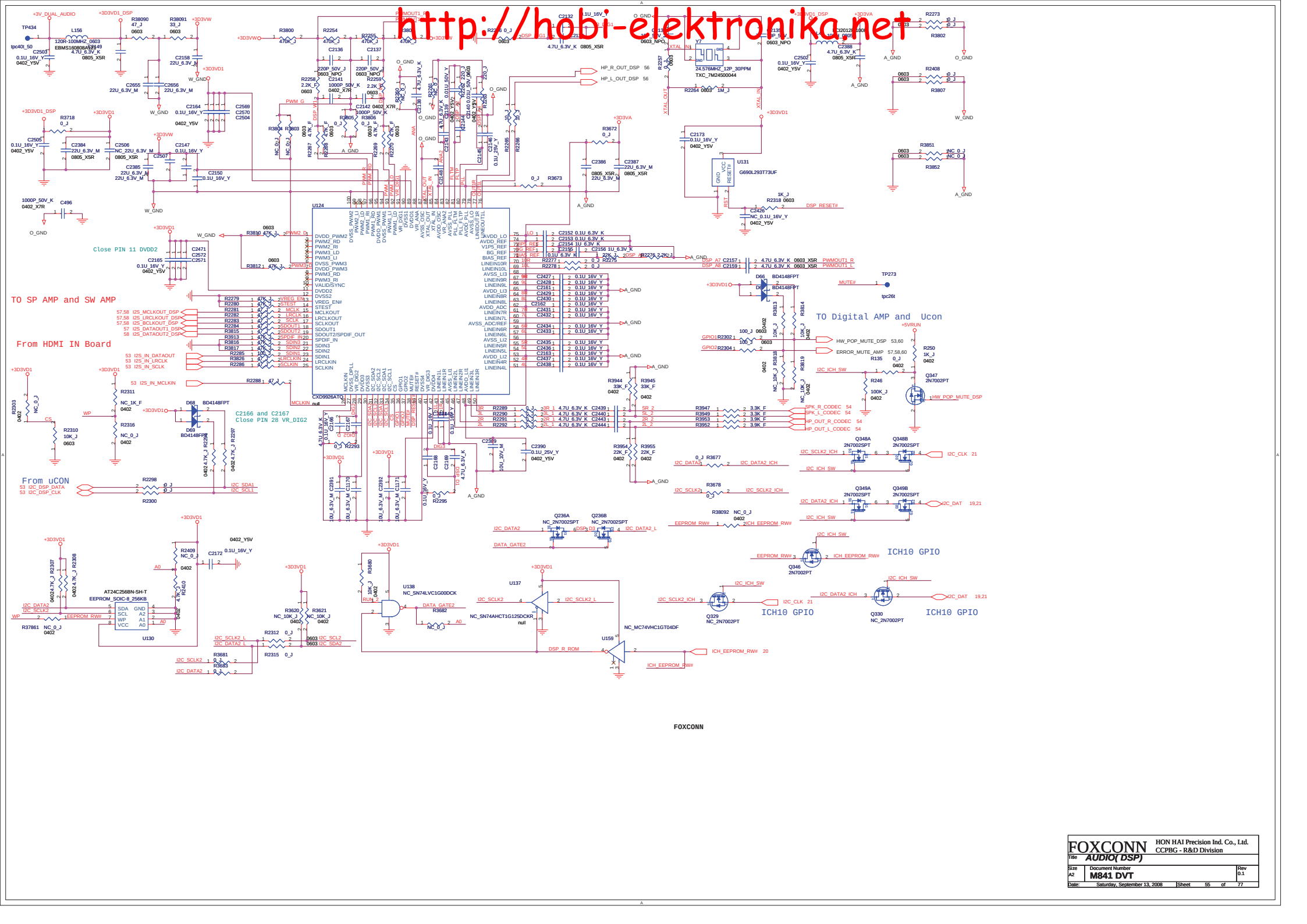

FOXCONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	AUDIO(DSP)
Size A2	Document Number M841 DVT
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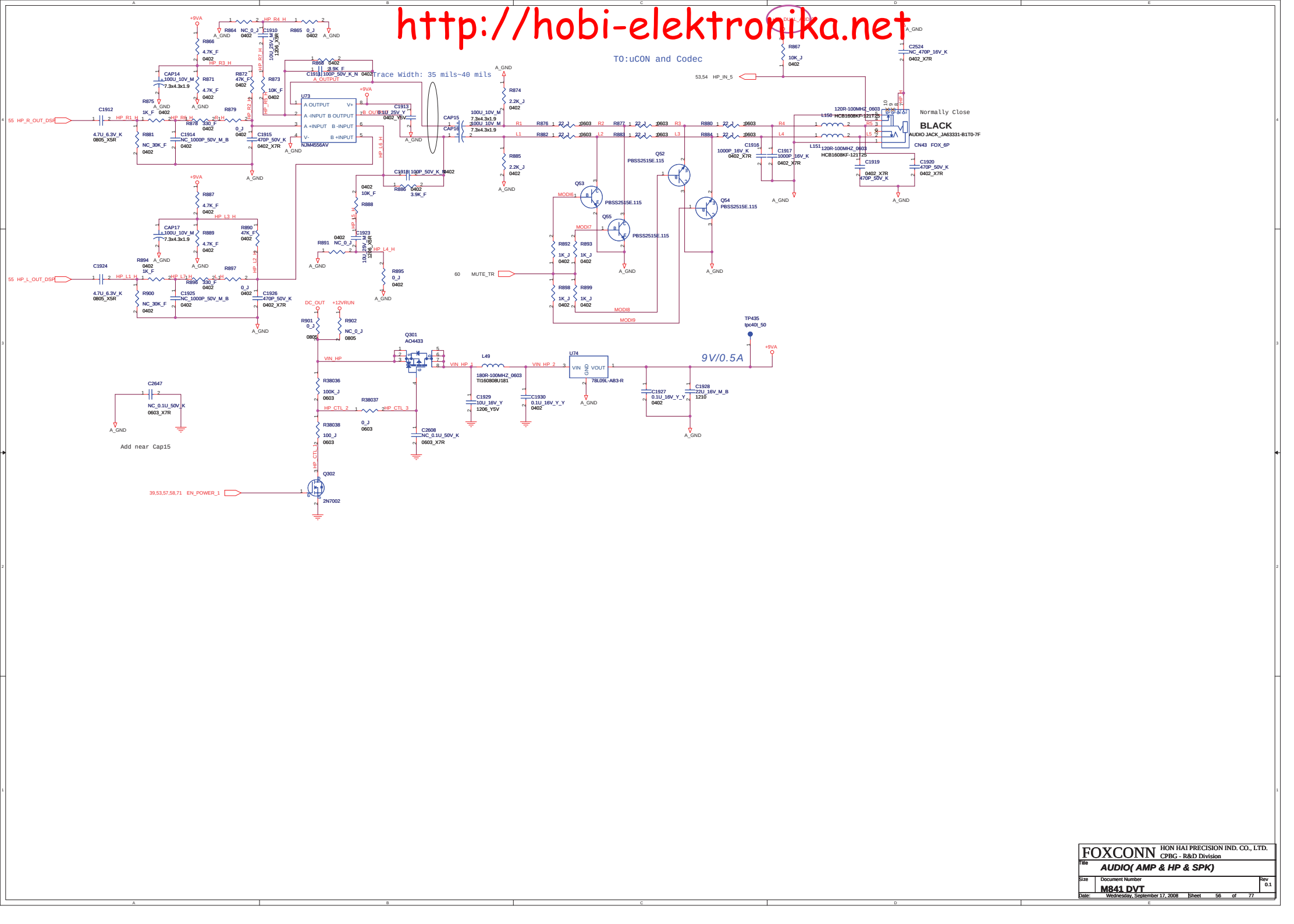

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	AUDIO(AMP & HP & SPK)		
Size	Document Number M841 DVT		Rev 0.1
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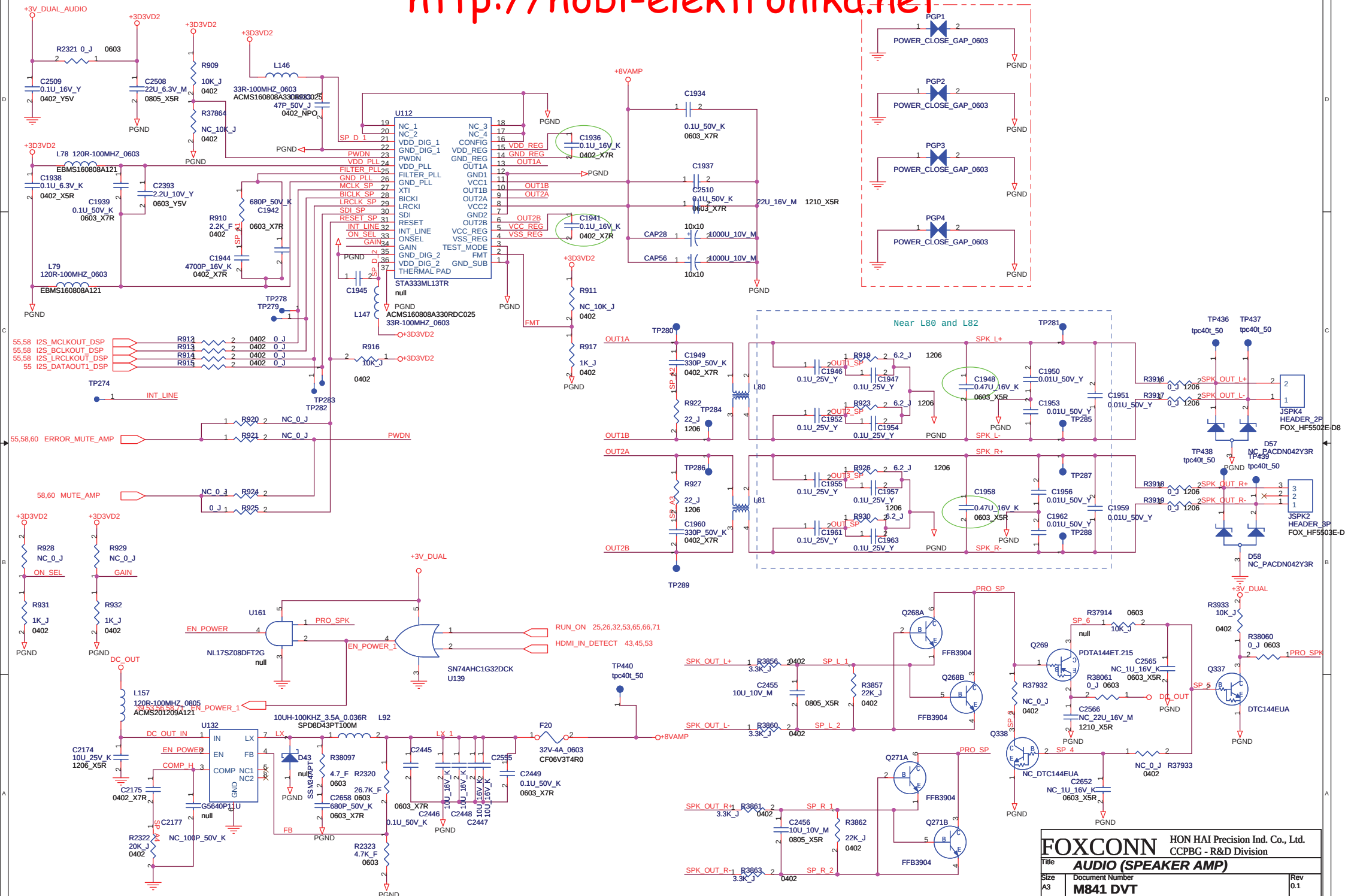

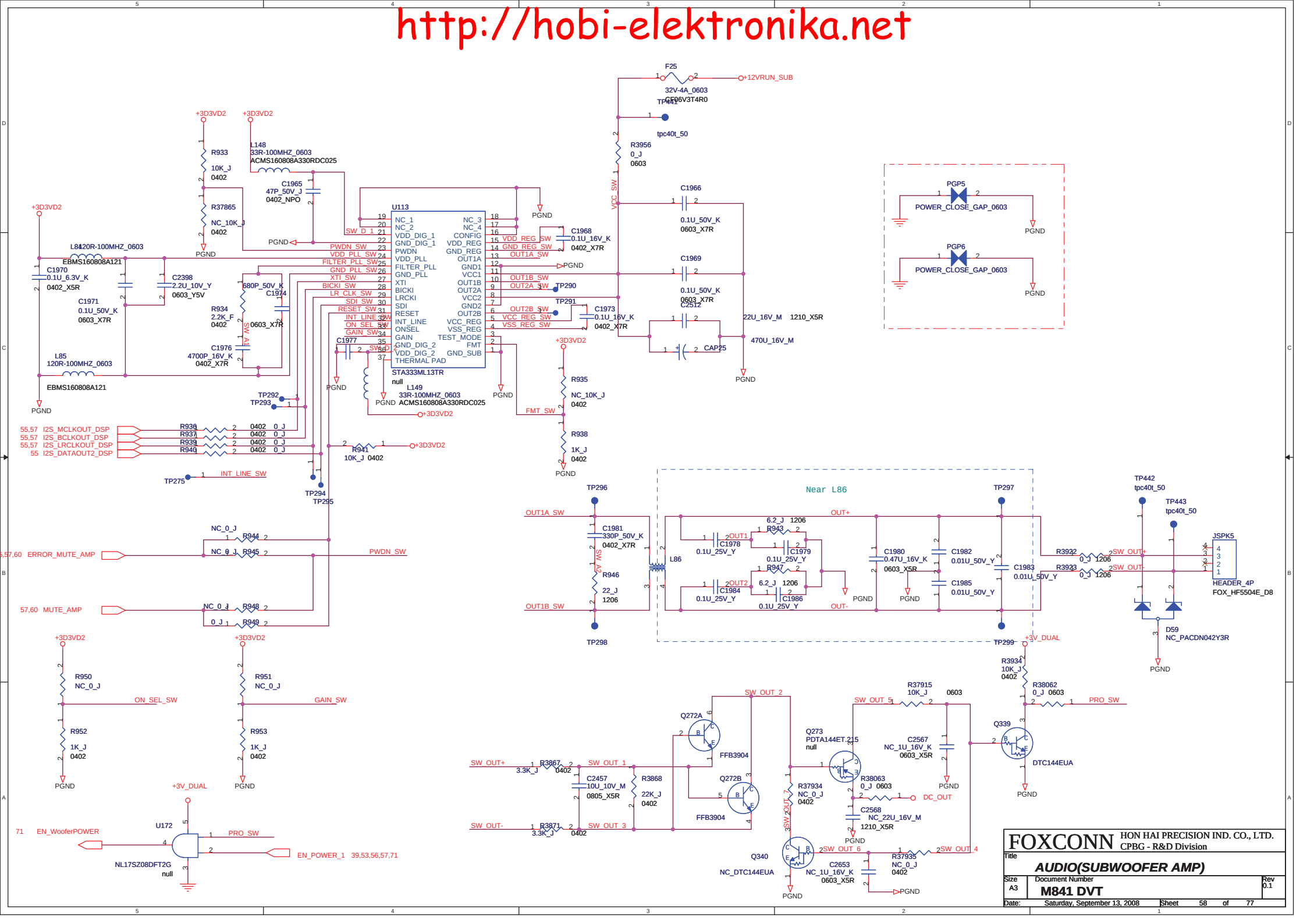

FOXCONN	HON HAI PRECISION IND. CO., LTD.	
	CPBG - R&D Division	
Title	AUDIO(SUBWOOFER AMP)	
Size A3	Document Number M841 DVT	Rev 0.1
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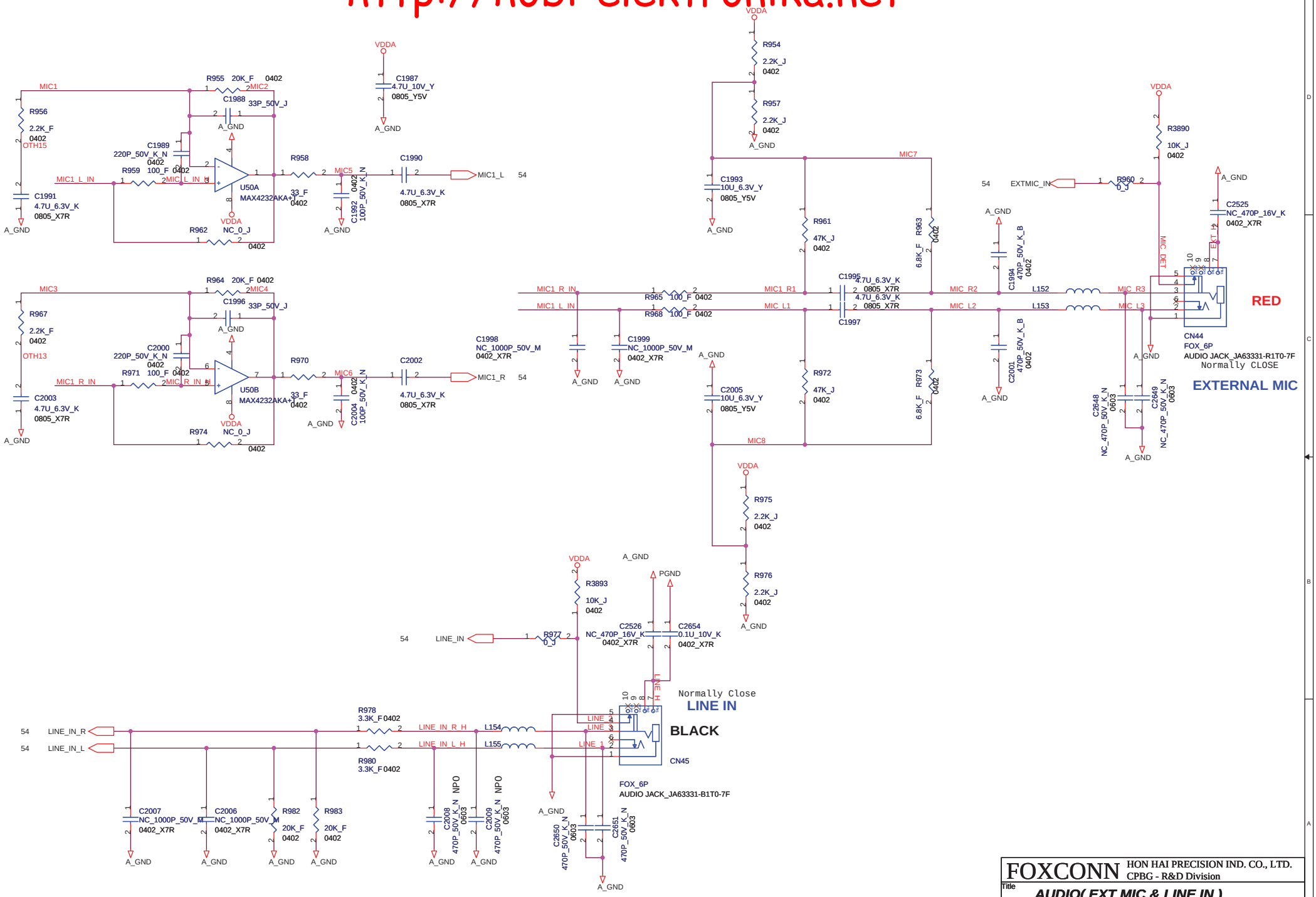

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	AUDIO(EXT MIC & LINE IN)		
Size A3	Document Number M841 DVT		Rev 0.1
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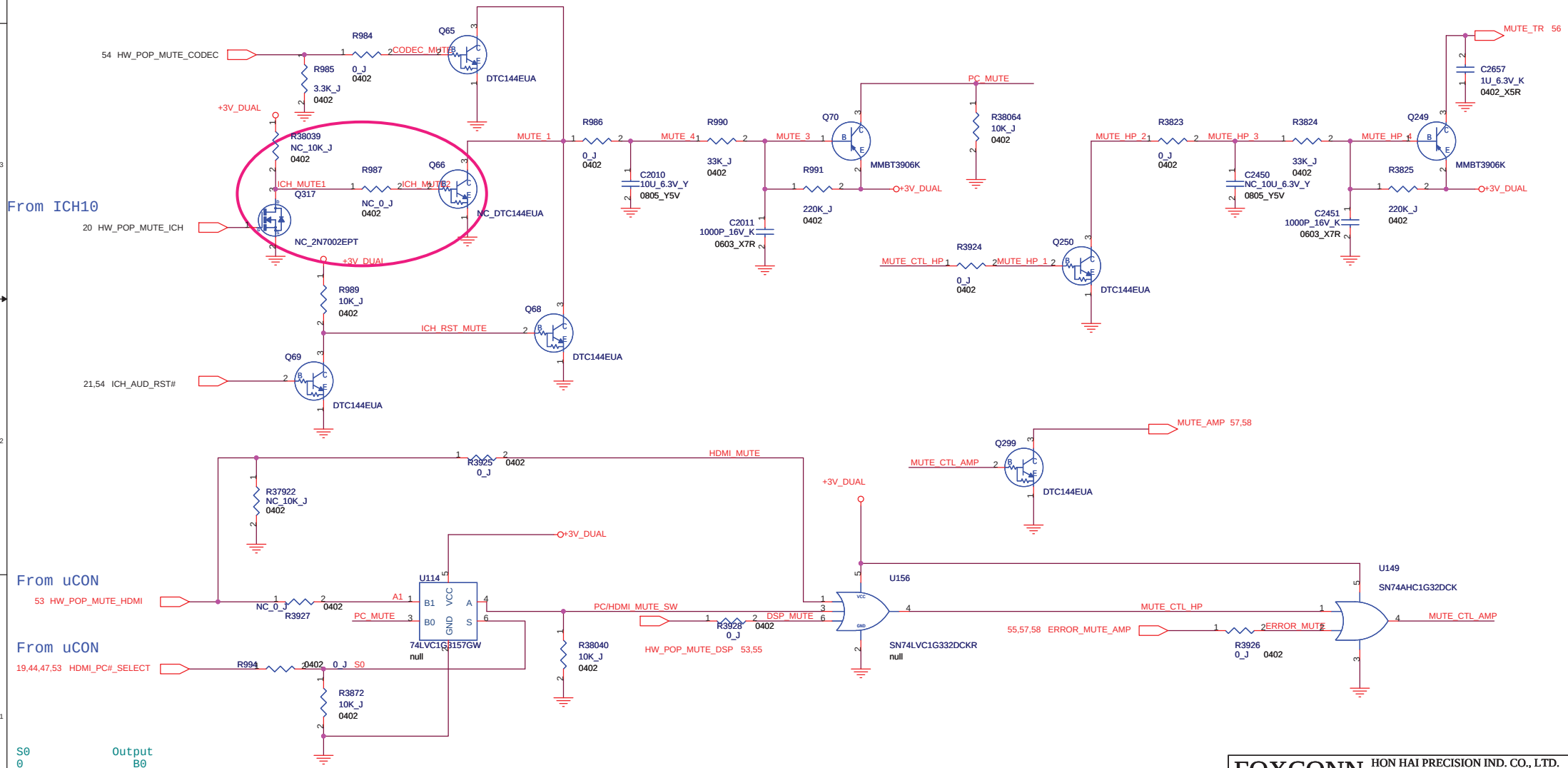
0829 NC Q317,R38039,R987,Q66 for cost down



S0 Output
0 B0
1 B1
When HIDEMI Mode ,HDMI/PC _Select pin is " 1"
When PC Mode , HDMI/PC_Select pin is "0"

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: AUDIO (MUTE)		
Size: A3	Document Number: M841 DVT	Rev: 0.1
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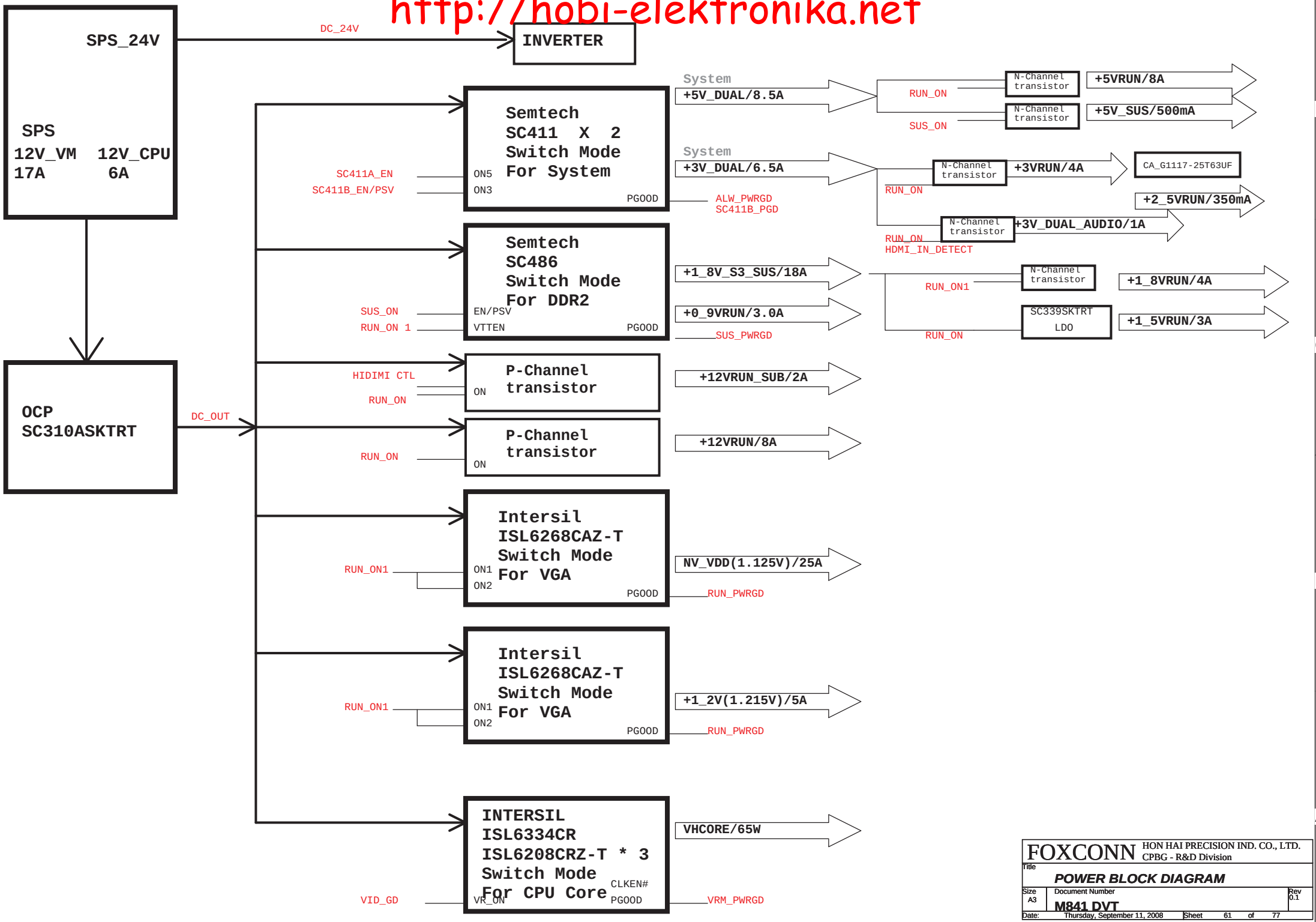

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: POWER BLOCK DIAGRAM

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37A

DC_IN / DC_OUT power plan should be great than 700mils

12V_VM
PTP46 tpc30t
PTP47 tpc30t
PTP48 tpc30t
PTP49 tpc30t
PTP50 tpc30t
PTP51 tpc30t
PTP44 tpc40t_75
PTP45 tpc40t_75
PTP52 tpc40t_75
PTP53 tpc40t_75
SPS_GND
DC_IN
DC_IN_R
DC_OUT
SPS_24V
DC_24V
+5V_AUX
SC310_IINP_HW
AC_OFF_3#
AOFF_3#X2
PURE_HW_SHUTDOWN#
PHS

PL12 60R-100MHZ_1806 BCMS451616A600 8A
PL13 60R-100MHZ_1806 BCMS451616A600 8A
PL14 60R-100MHZ_1806 BCMS451616A600 8A
PL15 60R-100MHZ_1806 BCMS451616A600 8A
PL16 60R-100MHZ_1806 BCMS451616A600 8A
PL17 60R-100MHZ_1806 BCMS451616A600 8A

PC1 0.01U_50V_M 0603_X7R
PC2 0.1U_50V_K 0603_X7R
PC3 0.1U_50V_K 0603_X7R
PC5 NC_10U_25V_M 1206_X5R
PC6 0603_X5R NC_1U_25V_M
PC7 NC_0.1U_50V_K 0603_X7R
PC10 0603_X5R NC_1U_25V_M
PC11 0.1U_50V_K_B 0603
PC14 0.1U_50V_K 0603_X7R
PC15 0.1U_50V_K 0603_X7R
PC16 0.1U_50V_K 0603_X7R
PC17 0.1U_50V_K_B 0603
PC76 NC_0.1U_50V_K 0603_X7R

PR270 100K_J 0603
PR272 100K_J 0603
PR11 100_J 0603
PR248 0.003_2W_F 7520

PQ1 AO4433
PQ2 AO4433
PQ6 2N7002PT

PU1 SC310ASKTRT
SHDN OUT
GND CS-
VCC CS+

Kelvin Pair

Vout=GAIN*ILoad*Rsense
For Total Power Dectect

PF4 125V-4A_6.1x2.69x2.69 R451004.MRL

PU4 78L05L-AB3-R
VIN GND VOUT
UTC78L05_IN
UTC78L05_OUT
+5V, 100mA
PR23 0_J 0603
PR24 0_J 0603
PC22 0.1U_50V_K_B 0603
PC23 4.7U_10V_K 0805_X5R

System over power protection set
AC_OFF_3# active at 110%

Total power 204W
PR19 =41.2K
PR25 =12K ==>224.4W

Control ACIN OCP protect

PR19 41.2K_F 0402
PR20 100K_J 0402
PR21 100K_J 0402
PR22 0_J 0402
PR25 12K_F 0402
PC18 1U_6.3V_M_B 0402
PC19 0.1U_16V_M 0402_X5R
PC20 0.1U_16V_M 0402_X5R
PC21 1U_6.3V_M_B 0402
PR18 0_J 0402
PR15 NC_0_J 0402
PR16 NC_10K_J 0402
PR17 NC_10K_J 0402

PU3 NCS2202SN1T1G
PQ9 PDTA144ET
PQ10 MUN5213DW1T1G
PQ8 NC_2N7002SPT
PD4 CHN222PT

PLMC-01
PLMC-02
PLMC-04
PLMC-05
PLMC-06
PLMC-22

42,45 PURE_HW_SHUTDOWN#

4/22 NC PR17 PR16 PR15 PQ8

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Title	DC-IN	
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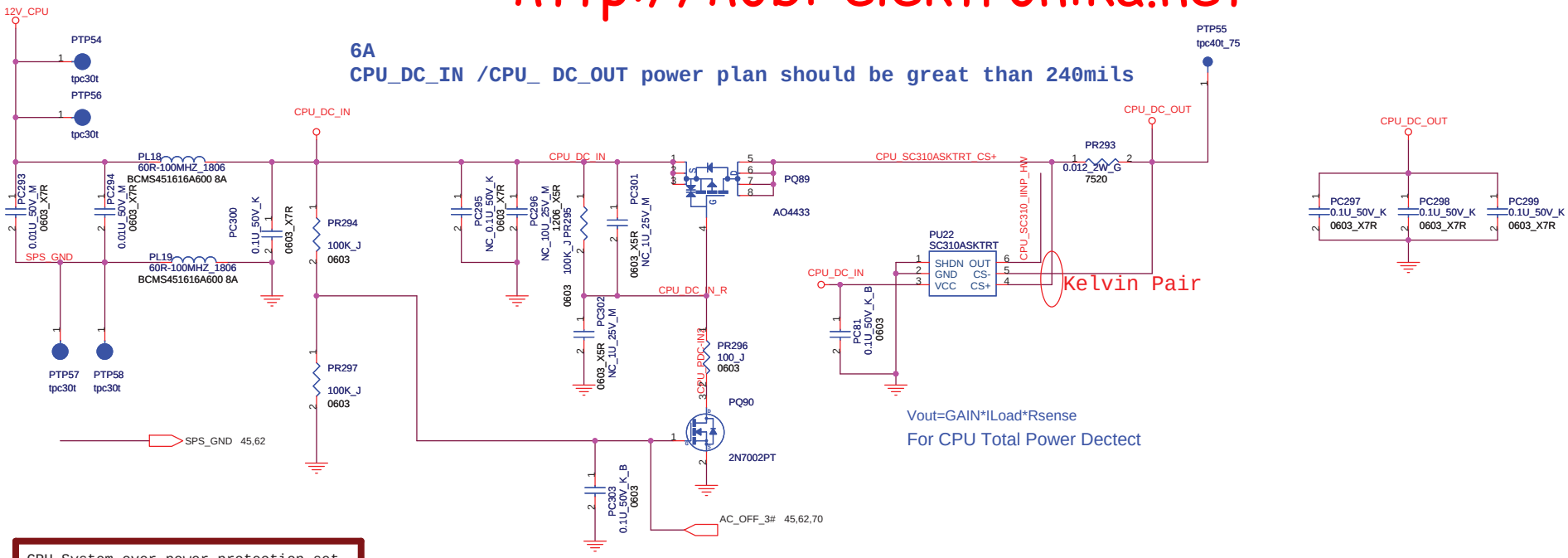
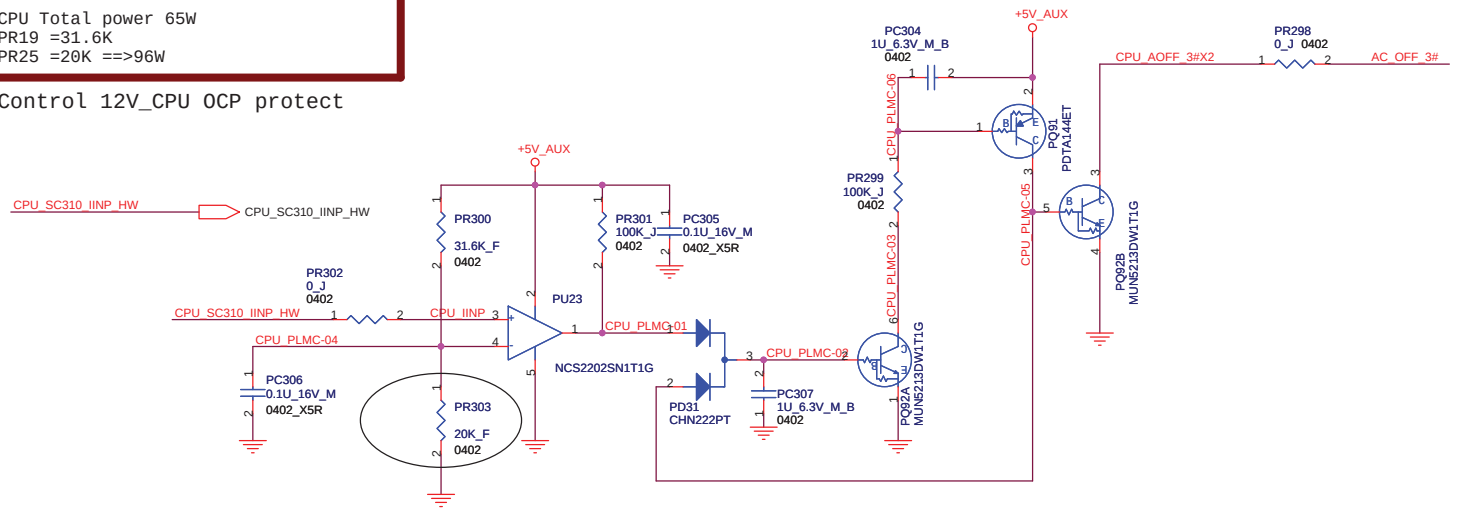


CPU System over power protection set
AC_OFF_3# active at 96W

CPU Total power 65W
PR19 =31.6K
PR25 =20K ==>96W

Control 12V_CPU OCP protect



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CPU_DC-IN	
Size A3	Document Number M841 DVT	Rev 0.1
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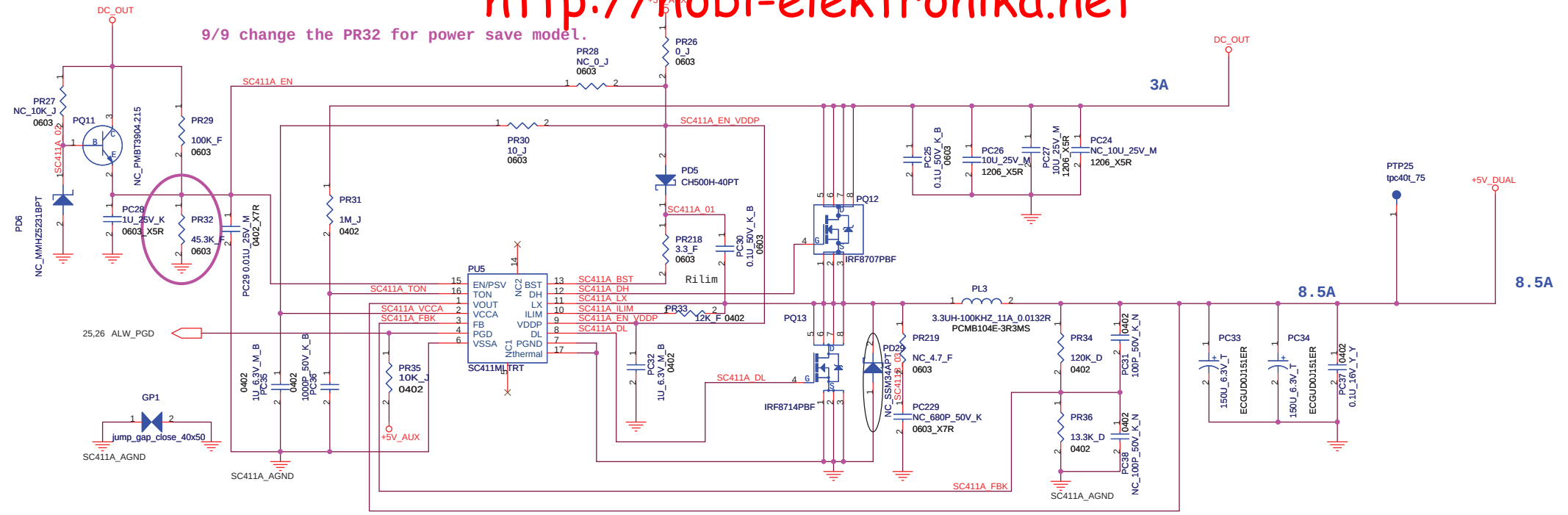
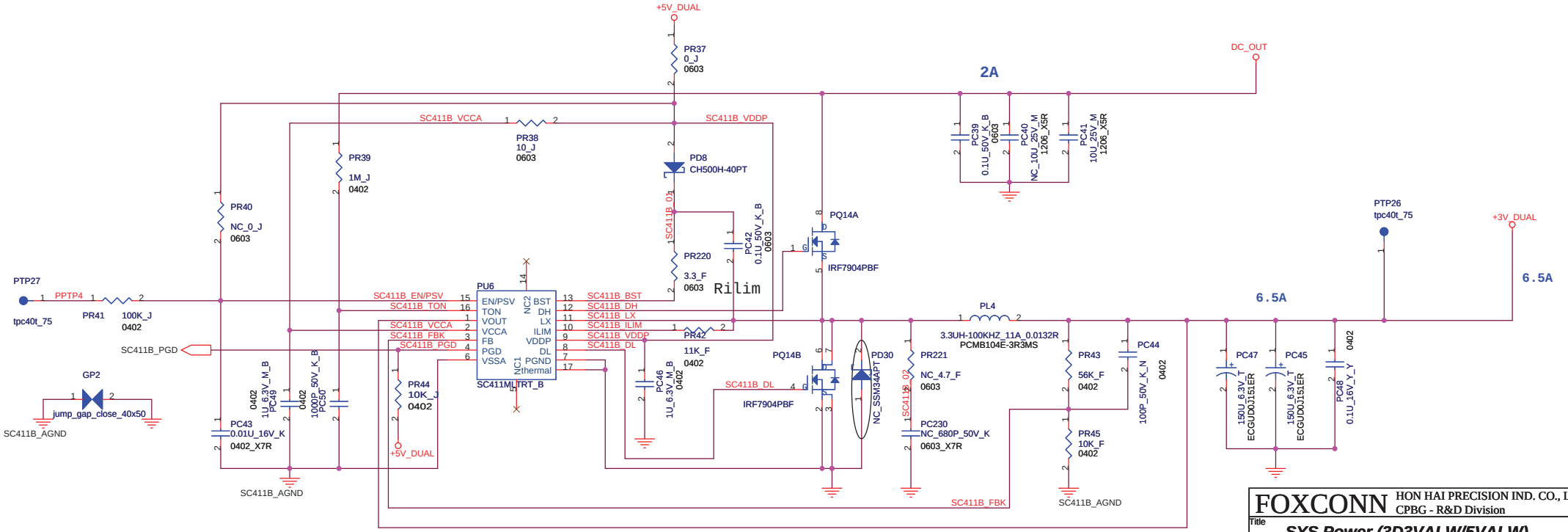
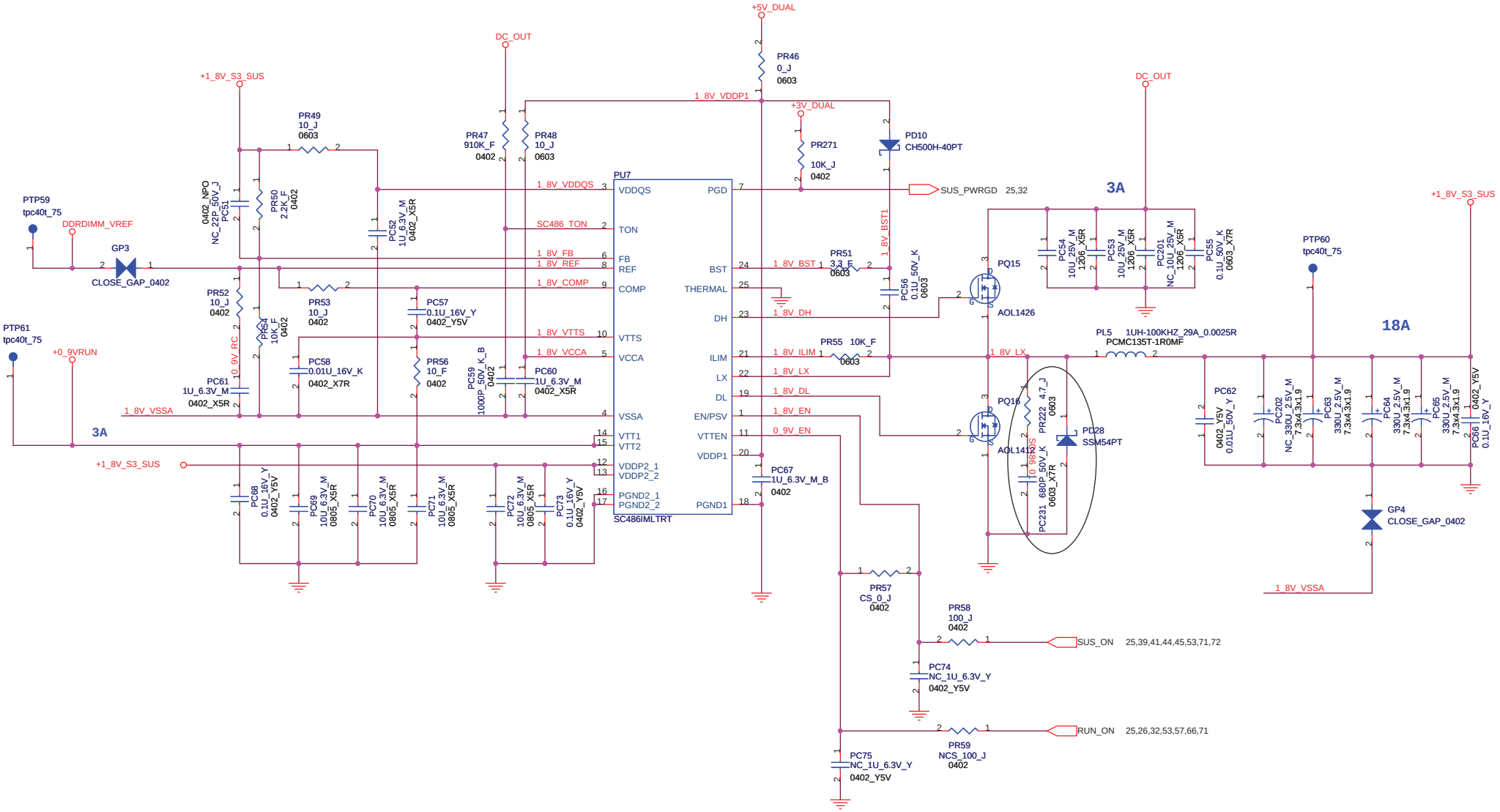
9/9 change the PR32 for power save model.

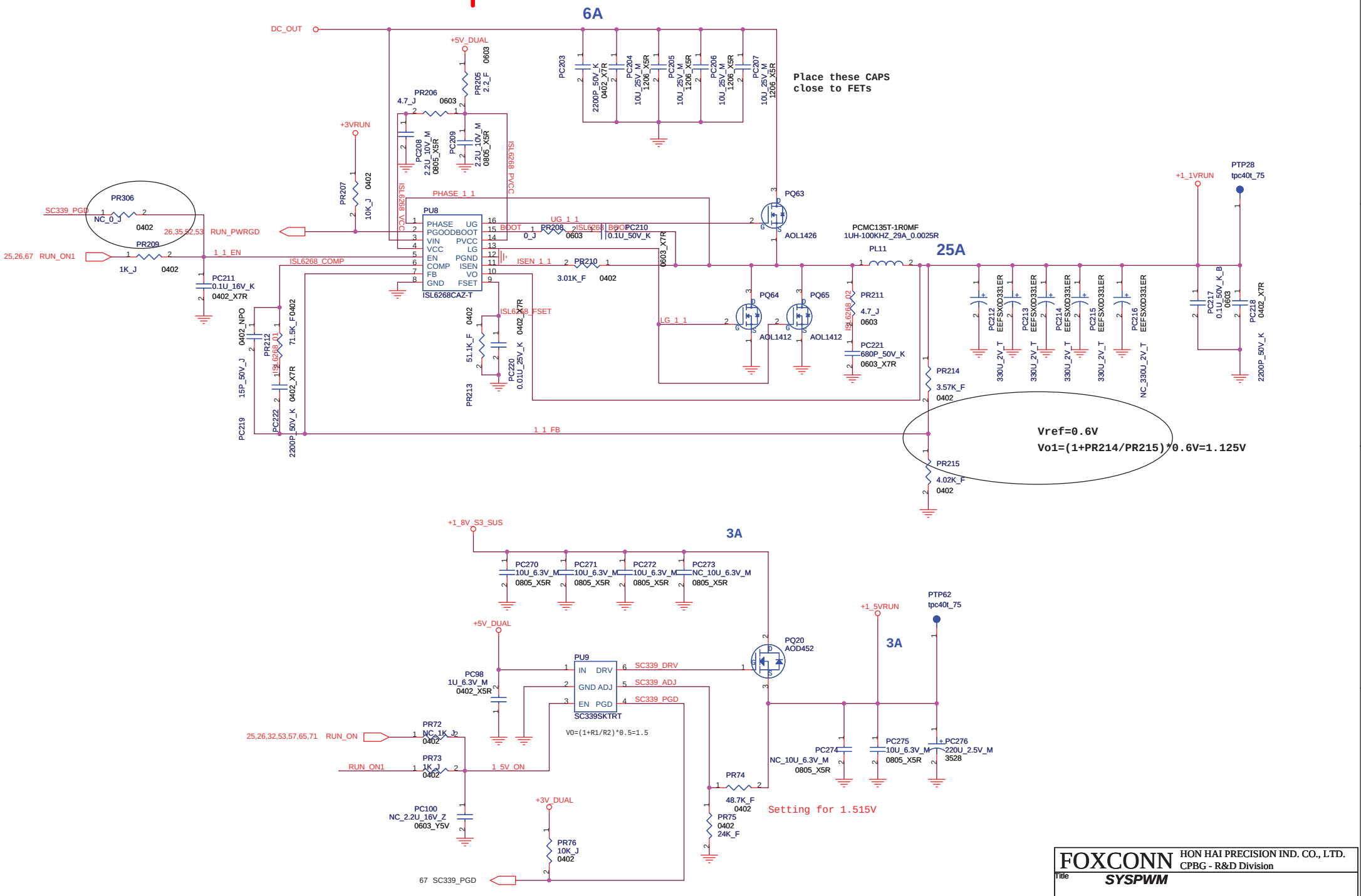




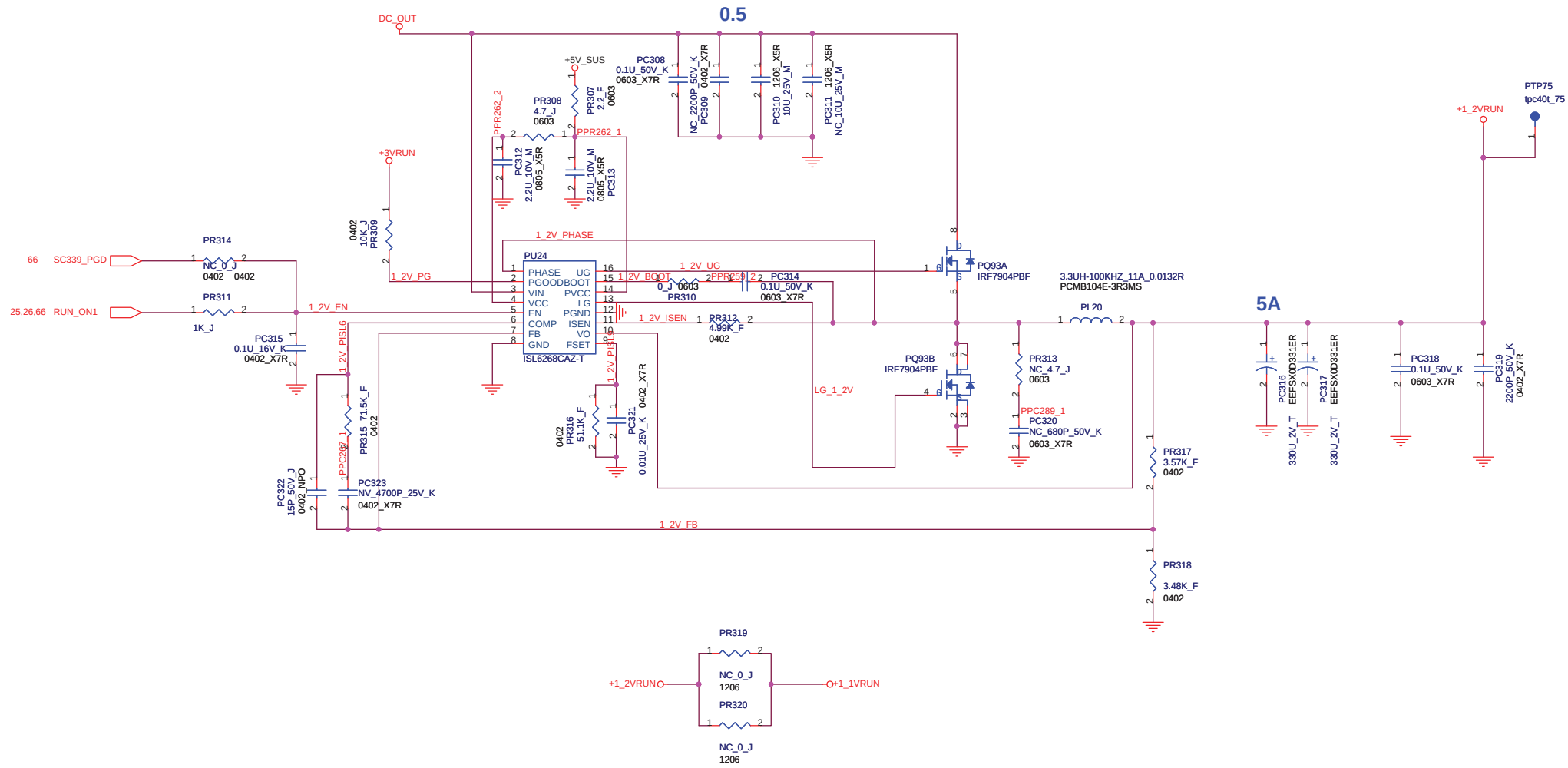
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SYS Power (3D3VALW/5VALW)	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Wednesday, September 17, 2008	Sheet 64 of 77	



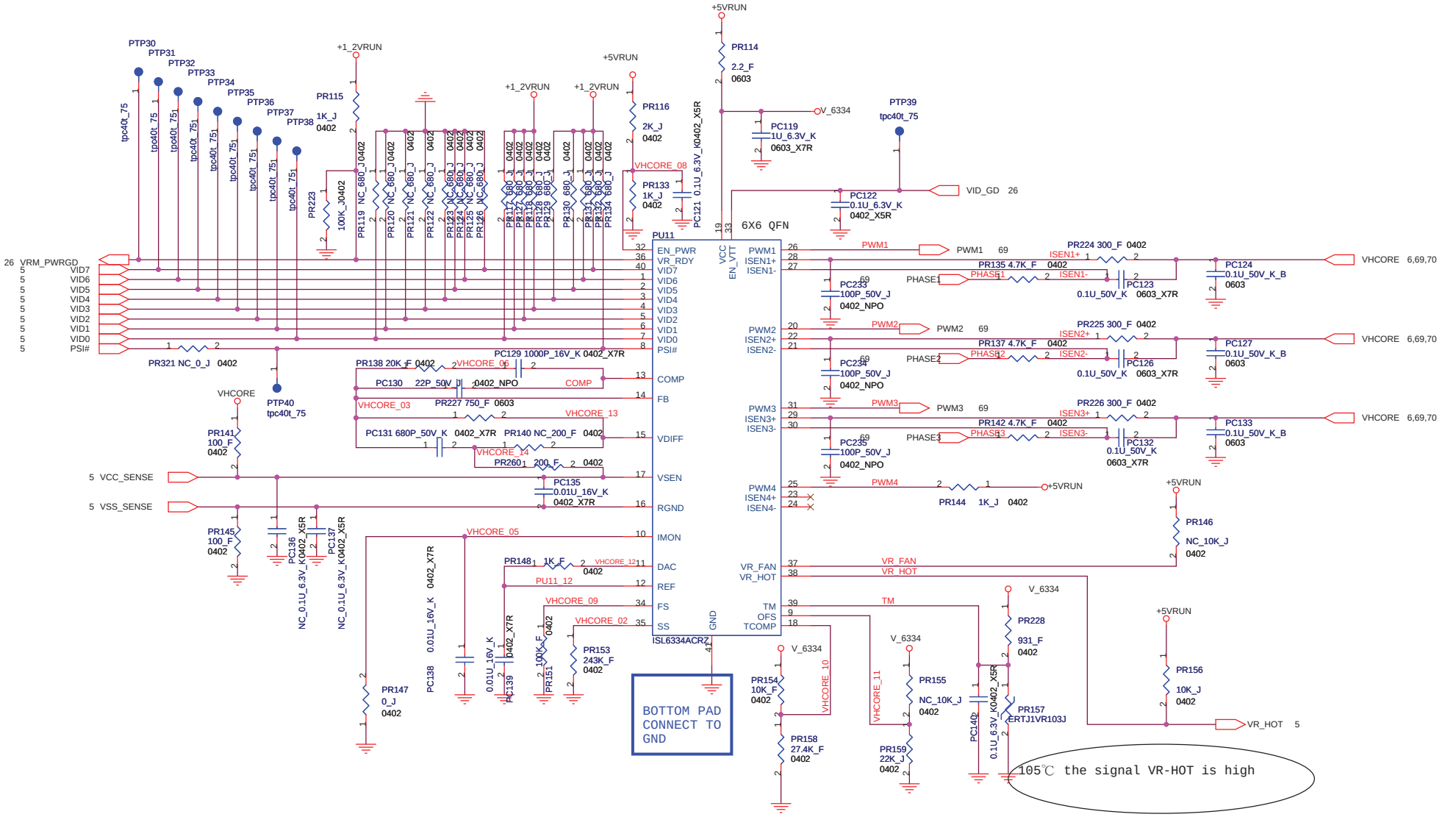
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2Power(+1_8V_S3_SUS/+0_9VRUN)	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 65 of 77	



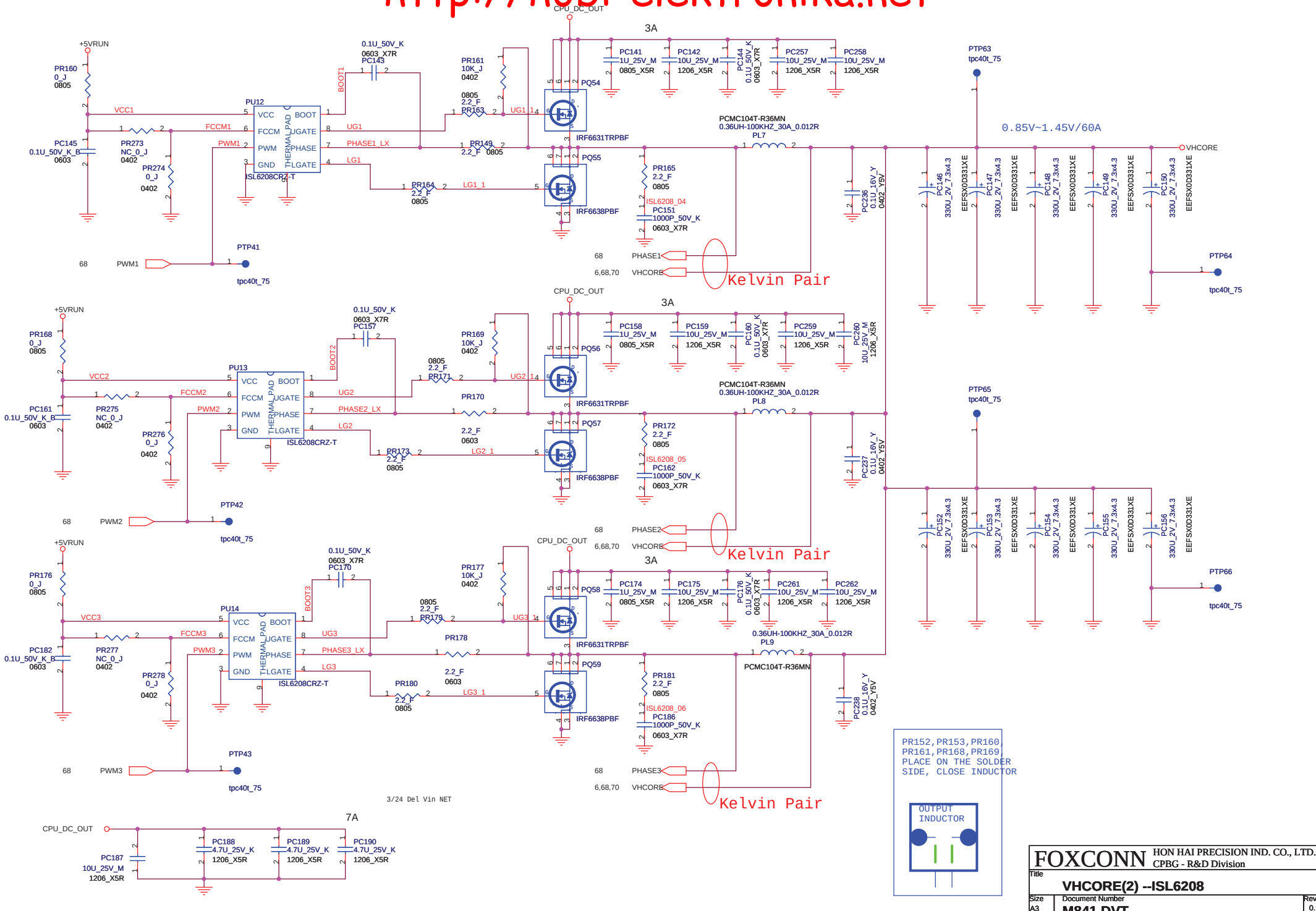
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SYSPWM	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 66 of 77	



Title	SYS Power (+1_2V)	
Size: A3	Document Number: M841 DVT	Rev: 0.1
Date: Saturday, September 13, 2008	Sheet 67 of 77	

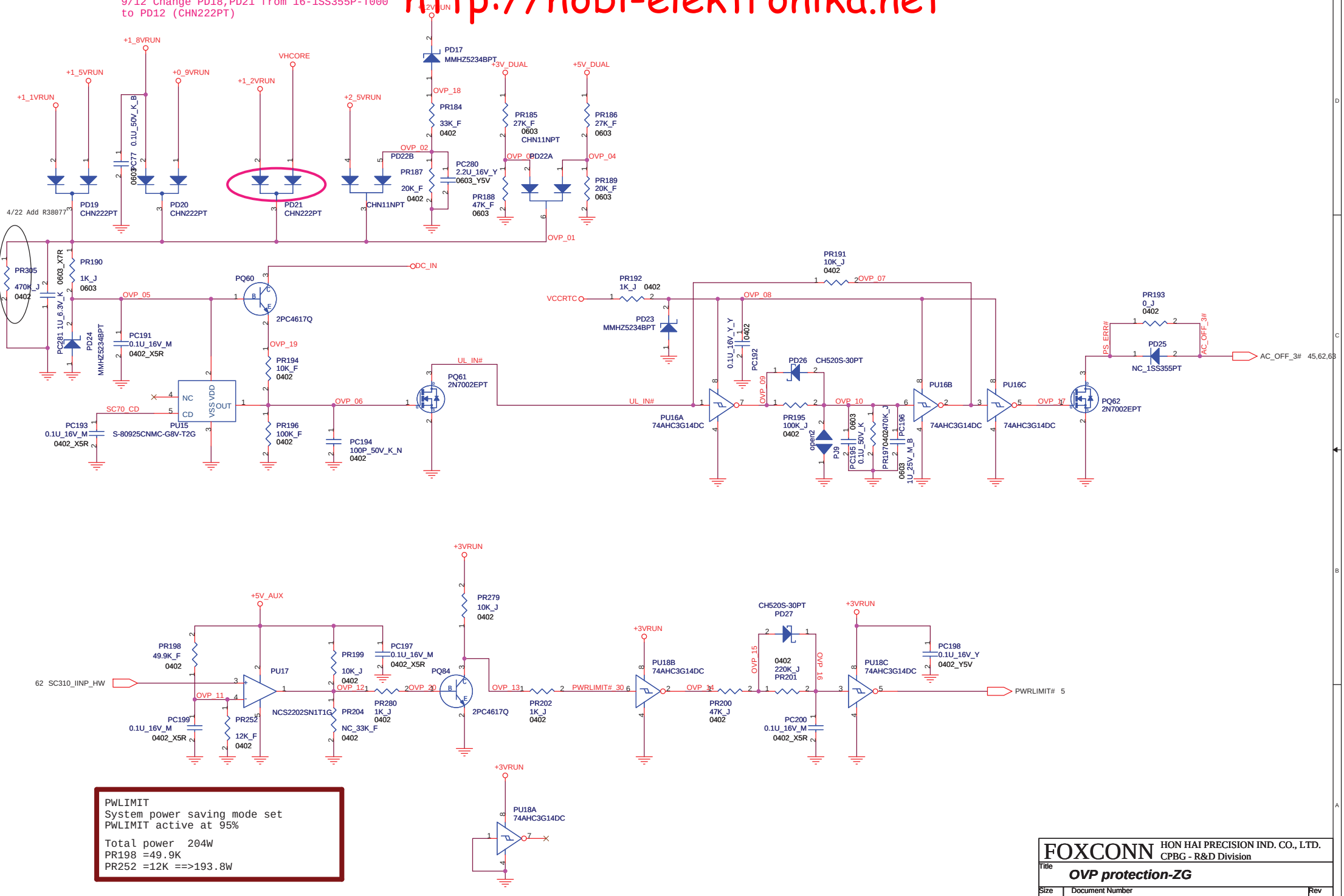


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	CHCORE (1)--ISL6334A
Size	A3
Document Number	M841 DVT
Rev	0.1
Date:	Saturday, September 13, 2008
Sheet	68 of 77



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VHCORE(2) --ISL6208	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Saturday, September 13, 2008	Sheet 69 of 77	

9/12 Change PD18,PD21 from 16-1SS355P-T000
to PD12 (CHN222PT)



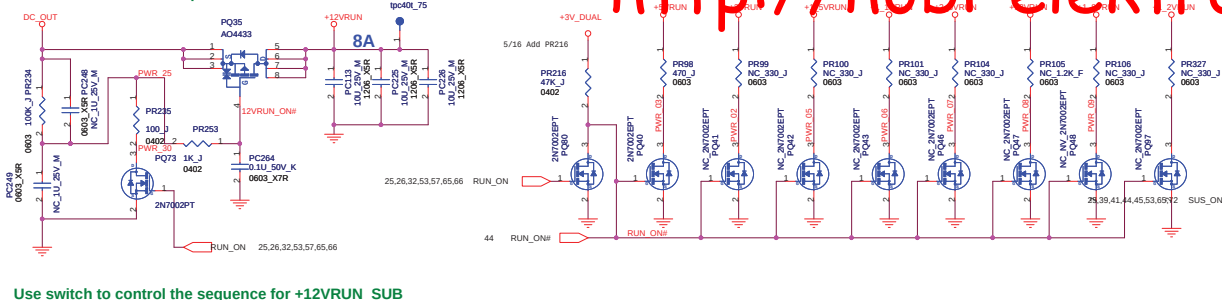
PWLIMIT
System power saving mode set
PWLIMIT active at 95%

Total power 204W
PR198 =49.9K
PR252 =12K ==>193.8W

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: OVP protection-ZG		
Size: A3	Document Number: M841 DVT	Rev: 0.1
Date: Wednesday, September 17, 2008	Sheet 70 of 77	

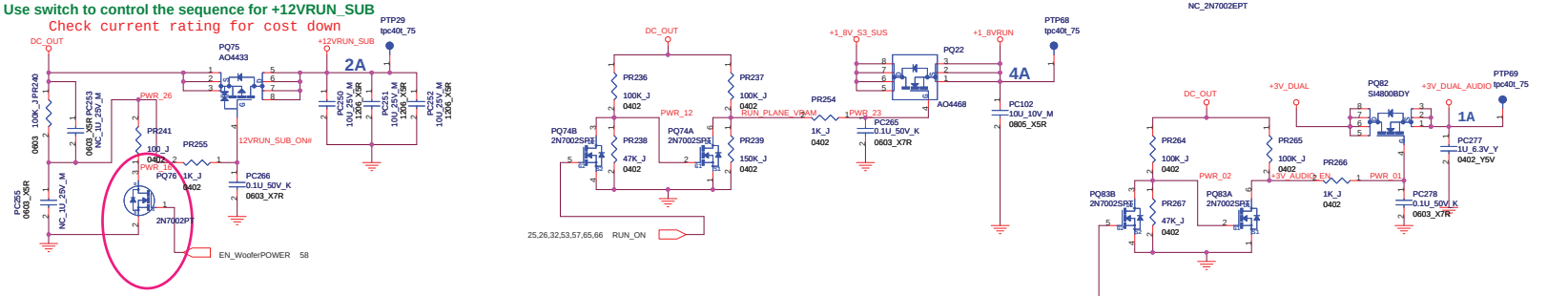
Use switch to control the sequence for +12VRUN

Discharge circuit

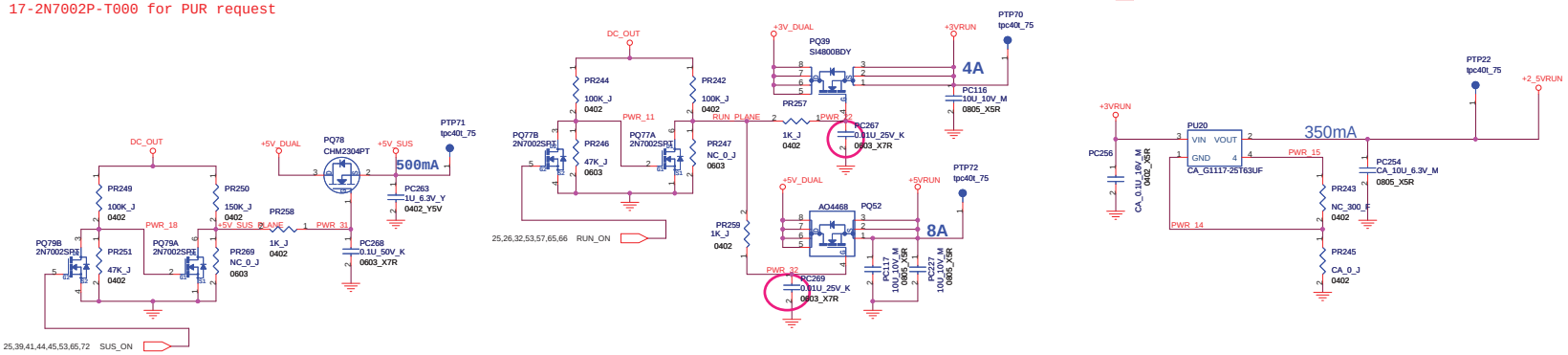


Use switch to control the sequence for +12VRUN_SUB

Check current rating for cost down

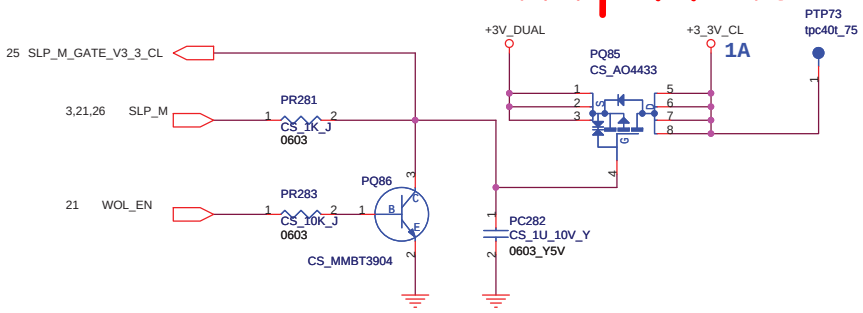


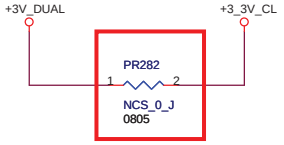
9/9 Change the PQ76 from 17-2N70020-0000 to
17-2N7002P-T000 for PUR request



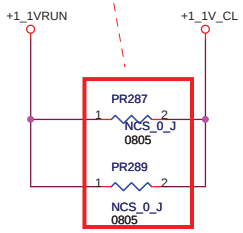
9/23 Change the PC267,PC269 from 1C-2B30104-K000(0.1u)
to 1C-2B30103-K000(0.01u) for new TV tuner Lyra

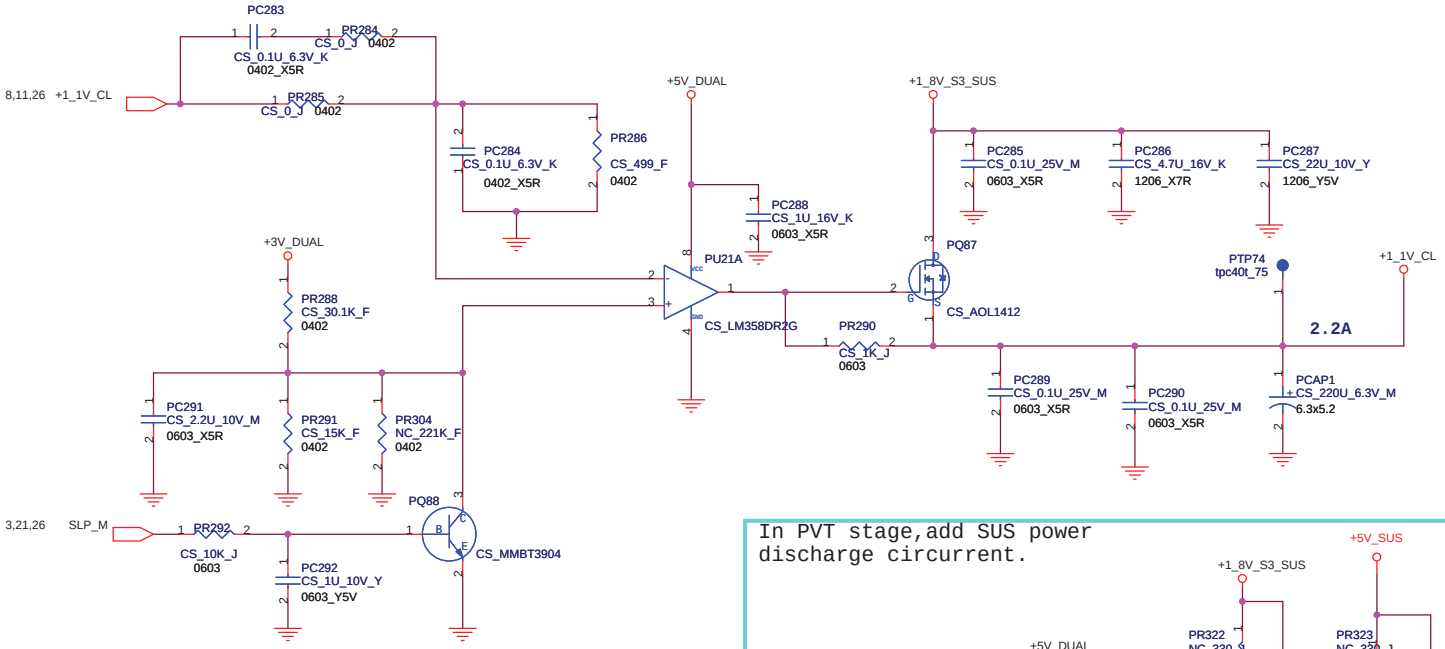
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Other power plan-ZG	
Size A2	Document Number M841 DVT	Rev 0.1
Date: Friday, September 26, 2008	Sheet 71 of 77	

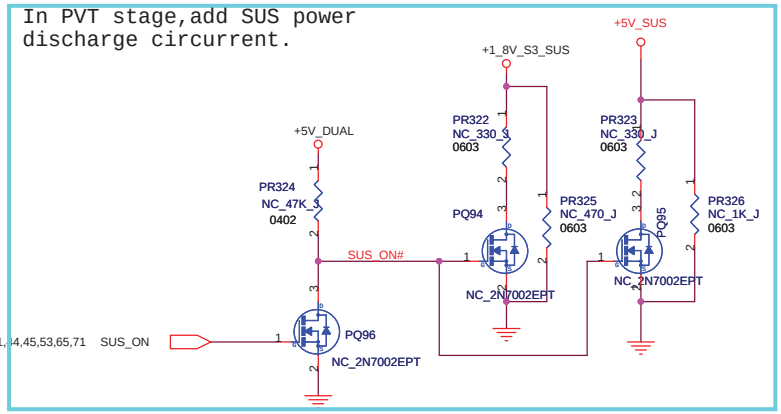




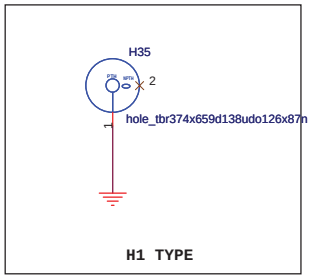
DVT:03/23:Default mount; NC for corwin spring.

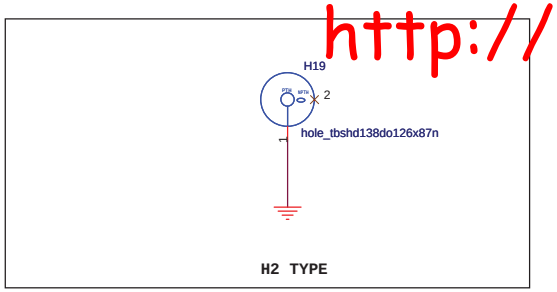


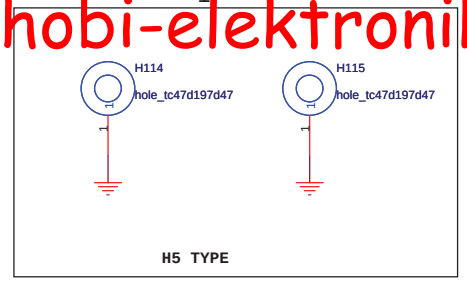


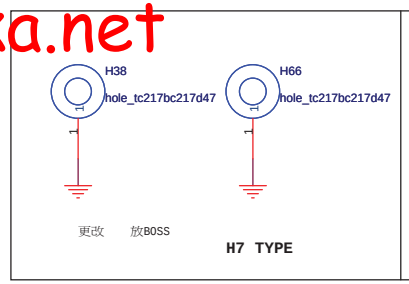


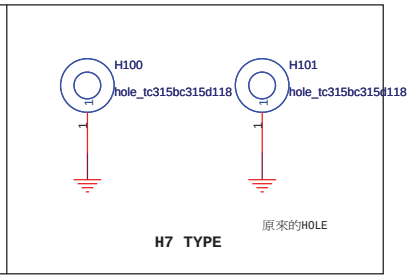
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *Corwin spring(3_3/1_1V_CL)*		
Size: A3	Document Number: M841 DVT	Rev: 0.1
Date: Saturday, September 13, 2008	Sheet 72 of 77	

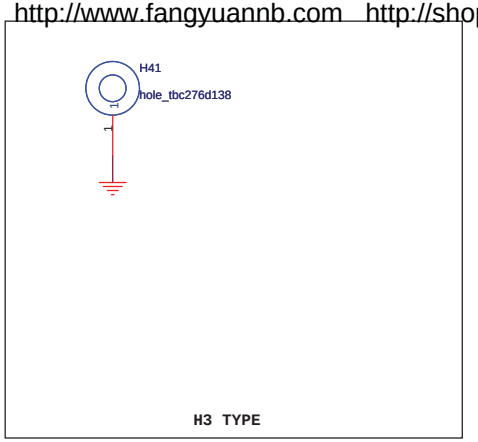


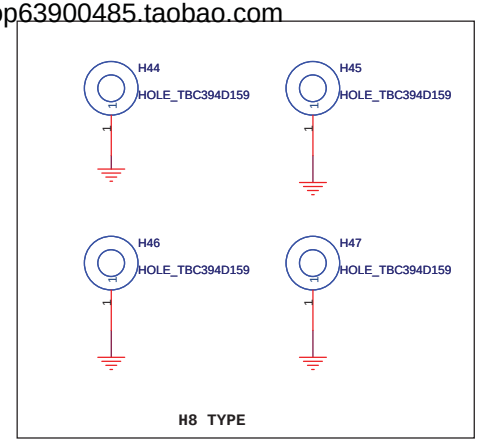


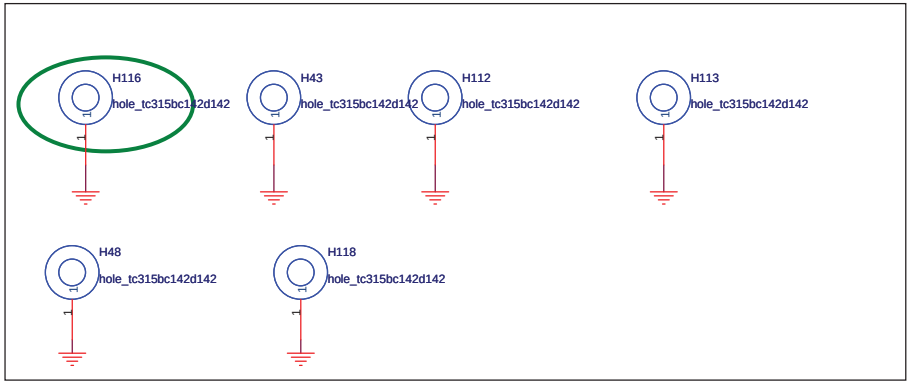


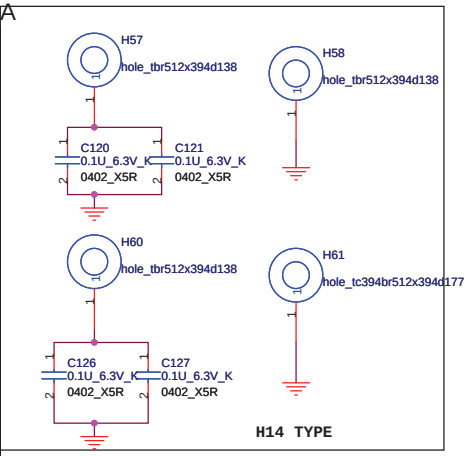


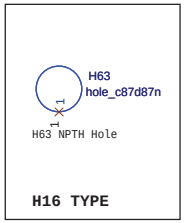


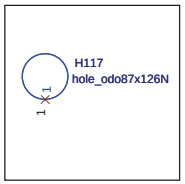


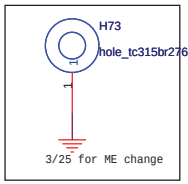


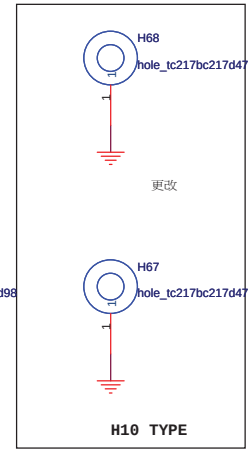


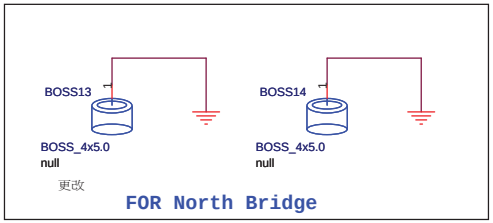


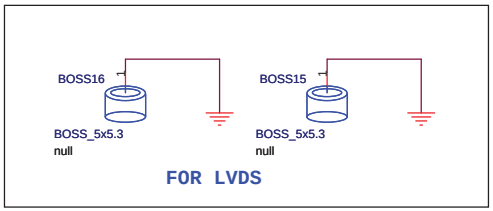




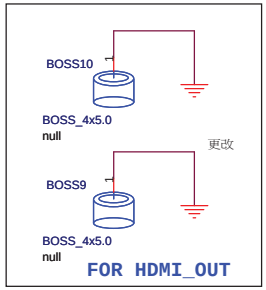


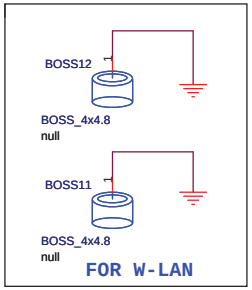


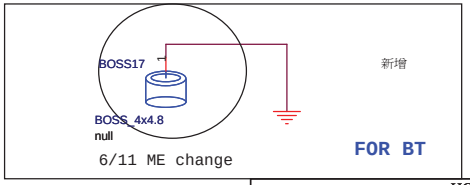




H9 TYPE







FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: HOLES & BOSS

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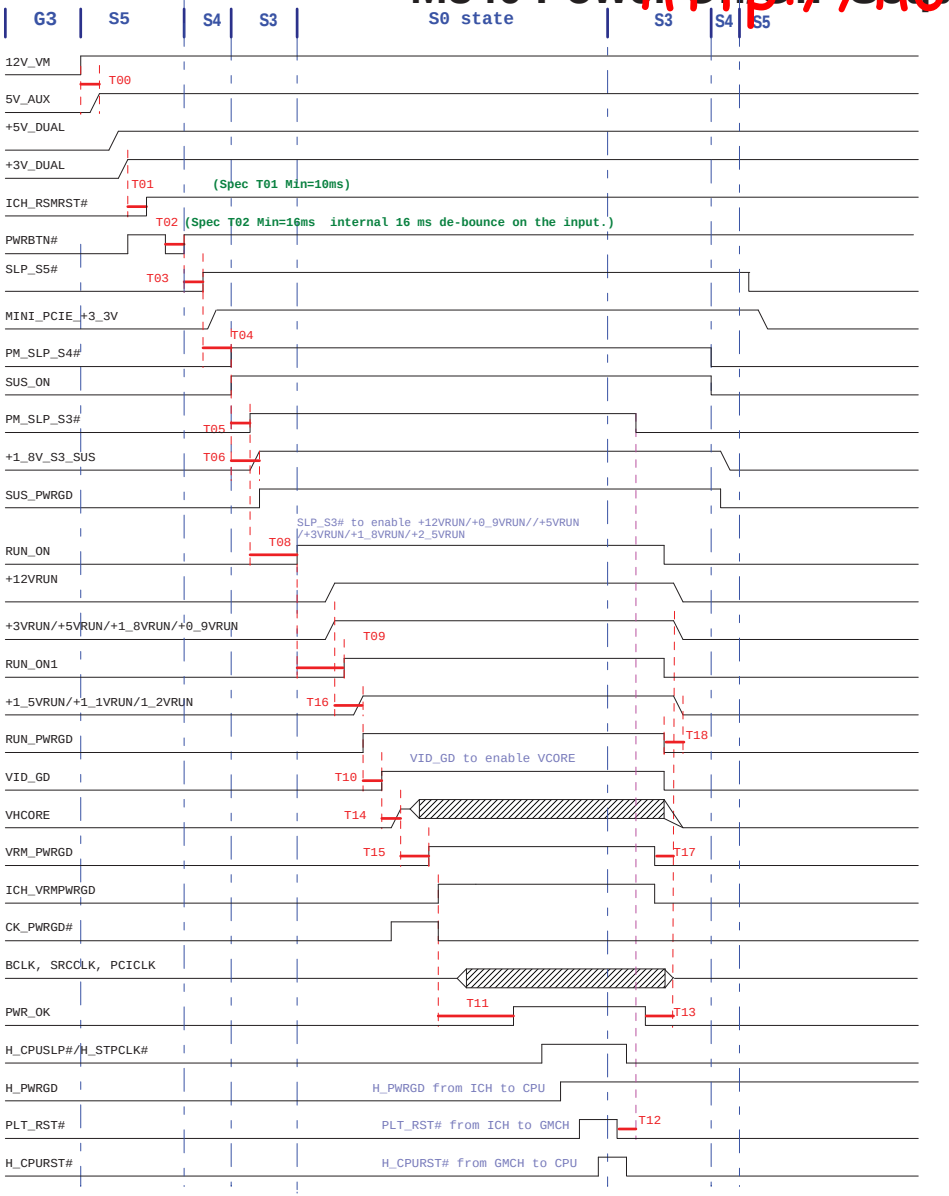
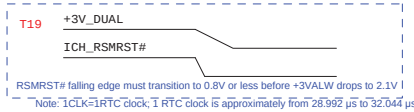
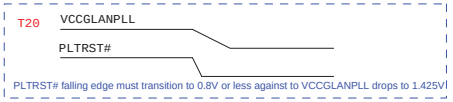
M840 Power On/Off Sequence Specification



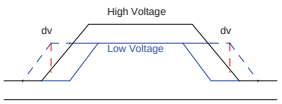




Note: 1CLK=1RTC clock, 1 RTC clock is approximately from 28.992 µs to 32.044 µs

	T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10	T11	T12	T13	T14	T15	T16	T17	T18	T19
Min	----	10ms	----	----	?CLK	?CLK	1CLK	----	60ms	10ms	30ms	99ms	1CLK	20ns	....	----	----	----	----	----
Typ	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----
Max	----	----	----	----	?CLK	?CLK	----	----	----	----	----	----	2CLK	----	----	----	----	----	----	----

High Voltage	V5REF (+5VRUN)	V5REF_SUS (+5V_DUAL)
Low Voltage	+3VRUN	+3VALW
dv	0.7V	0.7V
	Add Diode	



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **Power Sequence Timing**

Size: A2 | Document Number: **M841 DVT** | Rev: 0.1

Date: Friday, September 12, 2008 | Sheet 74 of 77

History (DVT)

2008/09/09

P71: Change the PQ76 from 17-2N70020-0000 to
17-2N7002P-T000 for PUR request

P64: Change the PR32 1R-0000203-F300 to 1R-0004532-F300
for power consumption

P20: For M841 SYS ID
Change R3901 from NC to stuff
Change R3774 from stuff to NC

P43: Add R38100,R38101for Q325 pin1 Q319 pin1 status

P44: Add R38102,LED9,Q350 for debug

2008/09/11

P54: Add R38102,LED9,Q350 for debug

P60 : NC Q317,R38039,R987,Q66 for cost down

P46 : Stuff CRT

Change CN53 pin assignment for HIDEMI,
change pin 12 from GND to SUS_ON;
change Pin 14 from GND to INV_BRADJ;
change Pin 40 from TP to INV_ENABLE1;
change Pin 39 from GND to HIDEMI_DETECT;
Add R38108 1M ohm for HIDEMI_DETECT PD.

P33 : Add F26(NC) for CF test debug

P53 : Add U178,R38110,R38111 back up circuit for
HIDEMI2 compatibility with HIDEMI 1 FW

2008/09/12

P30 : Change this circuit(U170,R37966,C2592,C2593,C2594,CN101,
R37967) from NC to stuff for EU TV tuner evaluation

P70 : Change PD18,PD21 from 16-1SS355P-T000
to PD12 (CHN222PT)

Page53: Add F27 for safety request

Page44: change CN86,R37898 from NC to stuff for use CRT for debug

Page27: L145 main soure change 1T-1NS6824-0300 to
1T-130F50L-0000(height:2.9mm),second source
1T-130F500-0000(height:2.5mm)

Page53: Add R38113(NC),R38114(stuff) , back up for HIDEMI debug

Page53: add 0 ohm R38115,R38116,R38117,R38118 at
HIDEMI_SUS_ON, LCDVCC_EN, INV_ENABLE1,
INV_BRADJ near HIDEMI connector

2008/09/23

P71 : Change the PC267,PC269 from 1C-2B30104-K000(0.1u)
to 1C-2B30103-K000(0.01u) for new TV tuner Lyra

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: Revision History(1)		
Size: A3	Document Number: M841 DVT	Rev: 0.1
Date: Tuesday, September 23, 2008	Sheet 75 of 77	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	**Revision History(2)**
Size: A3	Document Number: **M841 DVT**
Rev: 0.1	
Date: Thursday, September 11, 2008	Sheet 76 of 77

Title	Revision History(3)	
Size A3	Document Number M841 DVT	Rev 0.1
Date: Thursday, September 11, 2008	Sheet 77 of 77	